



# LDA2048P12.5S-1.7-T1

## Near-Infrared Linear Image Sensor (0.9 - 1.7 $\mu\text{m}$ ) with 2048 x 1 pixels

### FEATURES

- 2048 x 1 pixels [size: S 12.5  $\mu\text{m}$  x 12.5  $\mu\text{m}$ ]
- 28-pin Metal DIP Package
- Embedded Thermoelectric Cooler
- Built-in Temperature Sensor
- 0.9  $\mu\text{m}$  - 1.7  $\mu\text{m}$  Spectral Range
- Minimum Pixel Operability > 99 %
- Quantum Efficiency > 70 %
- Snapshot ITR / IWR
- 8 Outputs with a pixel rate of up to 22 MHz

### APPLICATIONS

- Shortwave-Infrared Imaging
- Hyper-, Multi-Spectral Imaging
- Semiconductor Inspection, Process Monitoring
- Sorting, Recycling



The LDA2048 is a near-infrared linear image sensor consisting of a linear InGaAs-detector array bonded to the p-on-n readout-IC. The product has a backup circuit function that can replace any of the 8 outputs.

## GENERAL DESCRIPTIONS

PARAMETER	UNIT	VALUE
Sensor Technology	---	Planar InGaAs PIN
Spectral Range	$\mu\text{m}$	0.9 - 1.7
Actual Pixel Array	---	2048 x 1
Pixel Pitch	$\mu\text{m}$	12.5
Pixel Size	$\mu\text{m}$	S: 12.5 x 12.5
Chip Size	mm	29.5 x 9.8
Package Type	---	28-PIN Metal DIP Package
Package Size L x W x T	mm	50.0 x 25.4 x 11.67
Weight	g	25.9



## SPECIFICATIONS (ITS<sup>1</sup> = 20 ± 1 °C)

PARAMETER	UNIT	TYPICAL VALUE	CONDITIONS	
Dark Current <sup>2,3</sup>	fA	S ≤ 150	Photo pixel biased @ - 0.5 V	
Quantum Efficiency <sup>2</sup> * Fill Factor (QEFF)	%	≥ 70	λ = 1550 nm	
Response Nonuniformity <sup>2</sup>	%	≤ 5	At 50% Full Well	
Response Nonlinearity <sup>2</sup>	%	≤ 2	15% - 85% Well Occupation Range	
Charge Capacity	Cint=6.4 fF Cint=16 fF Cint=30 fF Cint=120 fF Cint = 506.4 fF Cint = 1506.4 fF Cint = 2006.4 fF	μV/e <sup>-</sup>	16 settings from 6.4 fF to 2.1 pF	
				25
				10
				5.33
				1.33
				0.316
				0.106
Readout Noise	Cint=6.4 fF Cint=16 fF Cint=30 fF Cint=120 fF Cint = 506.4 fF Cint = 1506.4 fF Cint = 2006.4 fF	mV	ROIC Specifications	
				1.2
				0.8
				0.6
				0.5
				0.4
				0.3
Output Swing	V	1.8 V ± 0.2	Gain @16 fF (High Gain Mode)	
Minimum Integration Period	μs	5	ROIC Specifications	
Maximum Pixel Rate	MHz	22	ROIC Specifications	
Pixel Operability <sup>2</sup>	%	≥ 99	Percentage of Pixels with QEFF Deviation within ± 20 % (QEFF Mean)	

1. Readings from Integrated Temperature Sensor (ITS).
2. These items are defined for central effective pixel array (2048 x 1). Their values correspond to default operation conditions.
3. High gain, charge capacity @ 16 fF, integration time 5 ms.

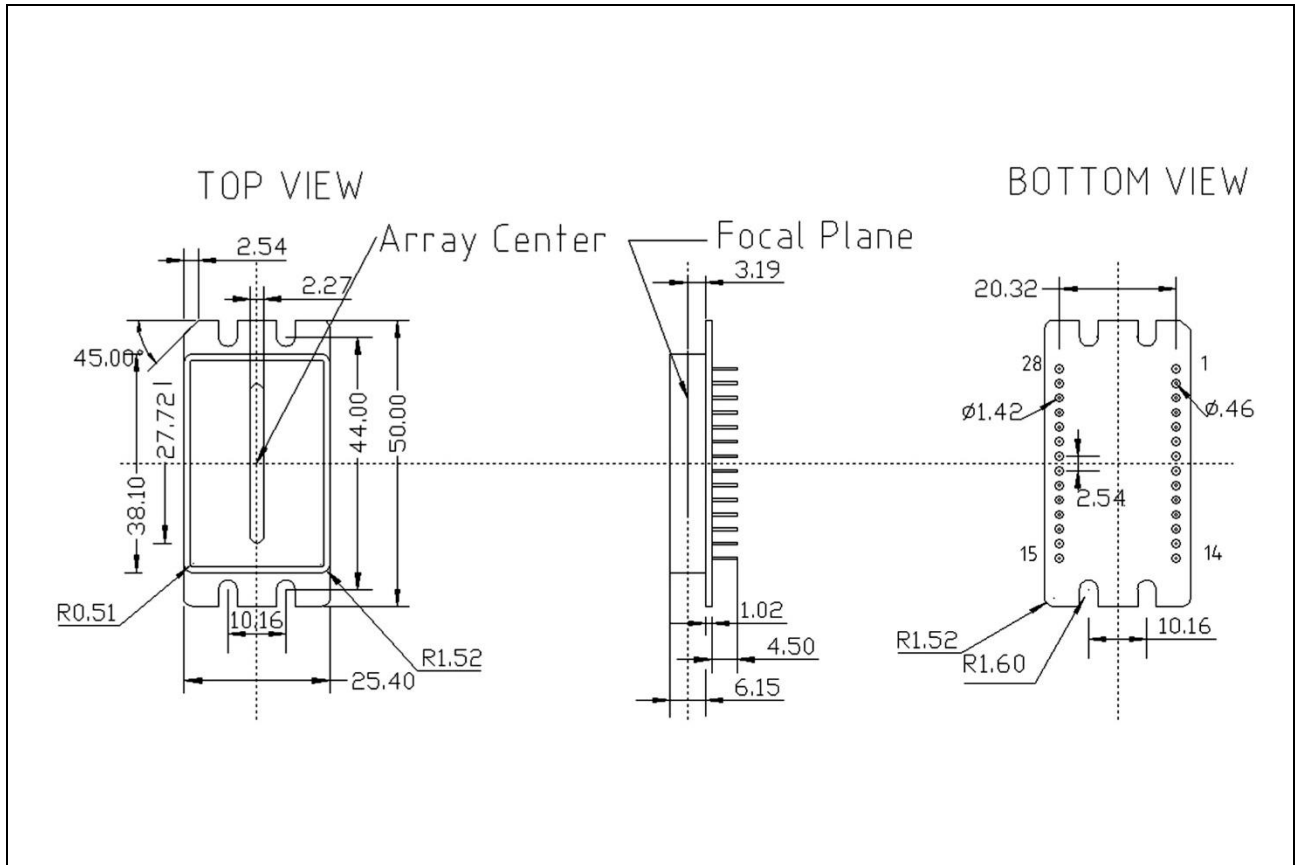
## ABSOLUTE MAXIMUM RATINGS

PARAMETER	UNIT	MIN.	MAX.
Operating Temperature <sup>4</sup>	°C	- 20	+ 70
Storage Temperature <sup>4</sup>	°C	- 40	+ 70
Power Consumption <sup>5</sup>	mW	---	190

4. In non-condensing environment.
5. Without powering on the thermoelectric cooler.



## PACKAGE OUTLINE (Unit: mm)



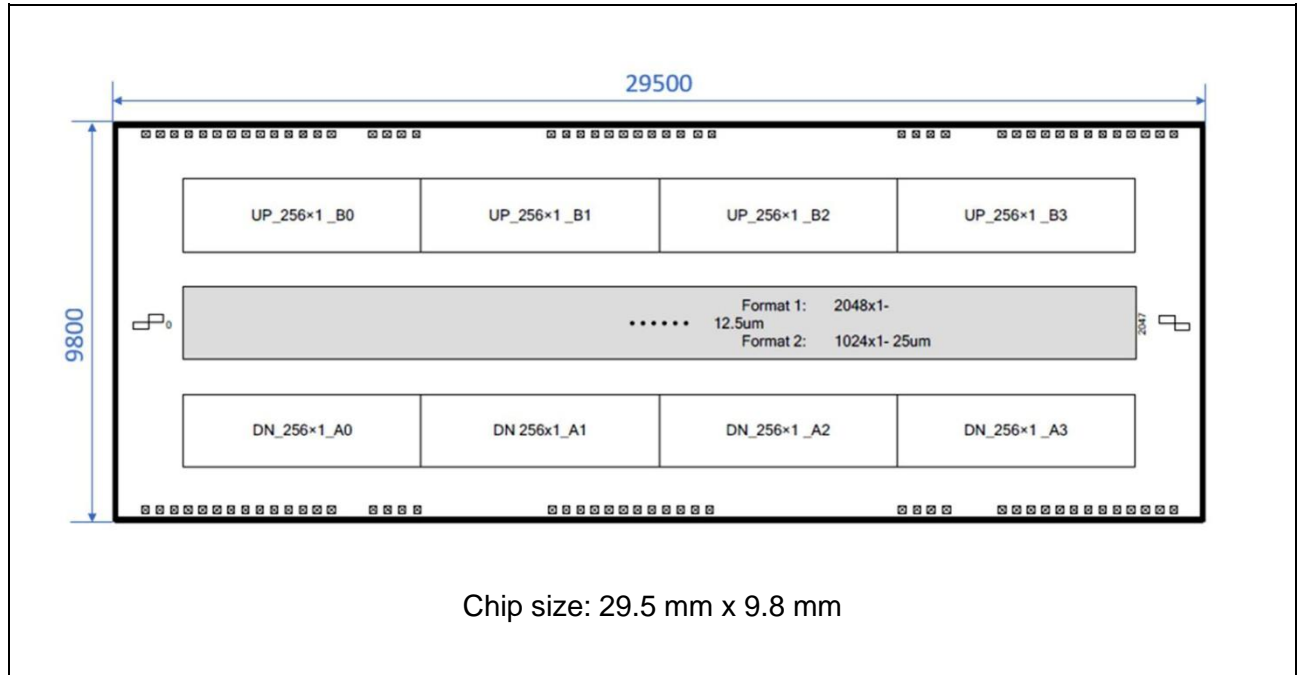
## PIN DEFINITION

01	TEC+	08	VTEMP	15	MC	22	SDOUT
02	VDETCOM	09	VOUT_0	16	INT	23	VOUT_7
03	VSSA	10	VOUT_2	17	CEB	24	VOUT_5
04	VDDA	11	VOUT_4	18	SDIN	25	VOUT_3
05	VR1	12	VOUT_6	19	VSS	26	VOUT_1
06	VR2	13	DATVALID	20	VDD	27	VDDAO
07	VOFFSET	14	RESET	21	DVDD	28	TEC-



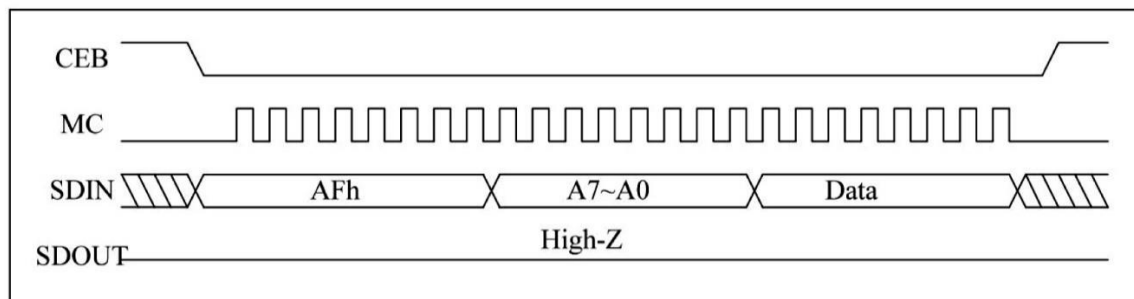
## CHIP PROFILE

### Layout



## SPI Interface

LDA2048P12.5S-1.7-T1 supports SPI protocol to set the command registers. There are functions of the gain mode, power consumption control and the sequence of pixel output.



SPI Protocol Schematic



## OPERATING CONDITIONS

### Bias Input

Pin #	Bias	Voltage	Current	Remark
01	TEC+	0 V ~ 3.1 V	< 2.4 A	Positive TEC Supply
28	TEC-	0 V	--	TEC Ground
02	VDETCOM	> VR1	--	Detector Common Voltage Detector Bias <sup>6</sup> = VDETCOM - VR1
04	VDDA	3.6 V	> 80 mA	Positive Analog Supply
05	VR1	2.3 V	> 30 mA	External Input Bias
06	VR2	0.3 V	> 40 mA	External Input Bias
07	VOFFSET	0.3 V ~ 2.3 V	> 40 mA	External Input Bias <sup>7</sup>
20	VDD	1.8 V	> 30 mA	Positive Digital Supply
21	DVDD	3.3 V	> 30 mA	Positive Digital Supply
27	VDDAO	3.6 V	> 80 mA	Positive Analog Supply
03	VSSA	0 V	--	Ground
19	VSS	0 V	--	Ground

6. VDETCOM lower than 2.3 V will forward bias the sensor, the exact zero bias voltage is device and temperature dependent.

7. OFFCLK\_EN=1'b0, VOFFSET function is not enabled; OFFCLK\_EN=1'b1 VR2 and VOFFSET realize offset voltage subtraction according to the working sequence.

### Digital Pattern Input

Pin #	Clocks	Levels	Rise / Fall	Remark
14	RESET	1.8 V	--	Chip Reset
15	MC	3.3 V / 0 V	< 5 nS	Master Clock, Max. Freq. = 22 MHz
16	INT	3.3 V / 0 V	< 50 nS	Integration Time
17	CEB	1.8 V / 0 V	< 10 nS	Chip Enable <sup>8</sup>
18	SDIN	3.3 V / 0 V	< 5 nS	Data Code Input

8. The input and output of all commands start after the falling edge of CEB.

### Digital Pattern Output

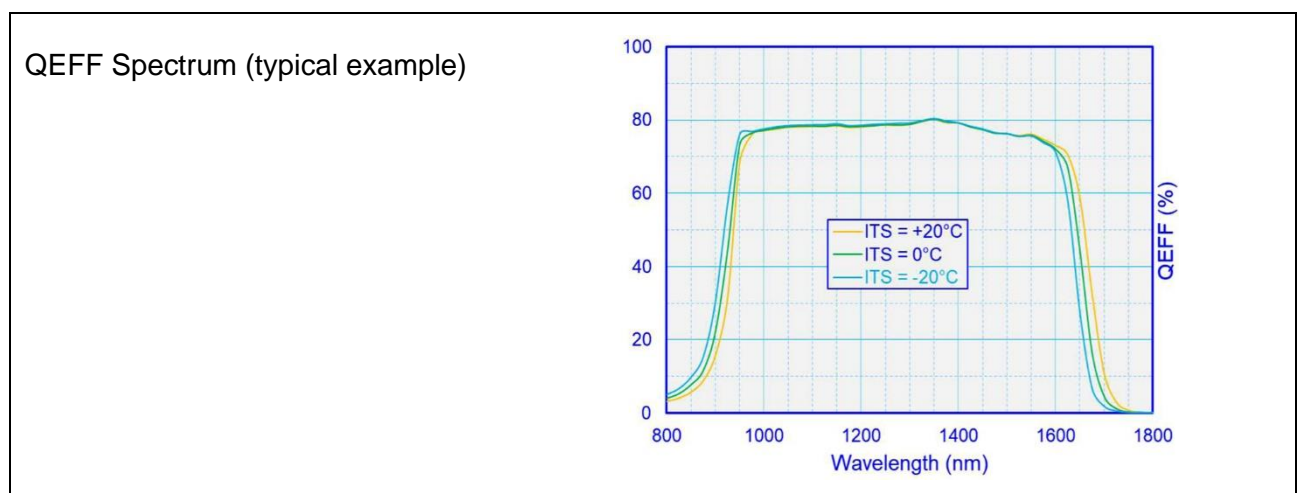
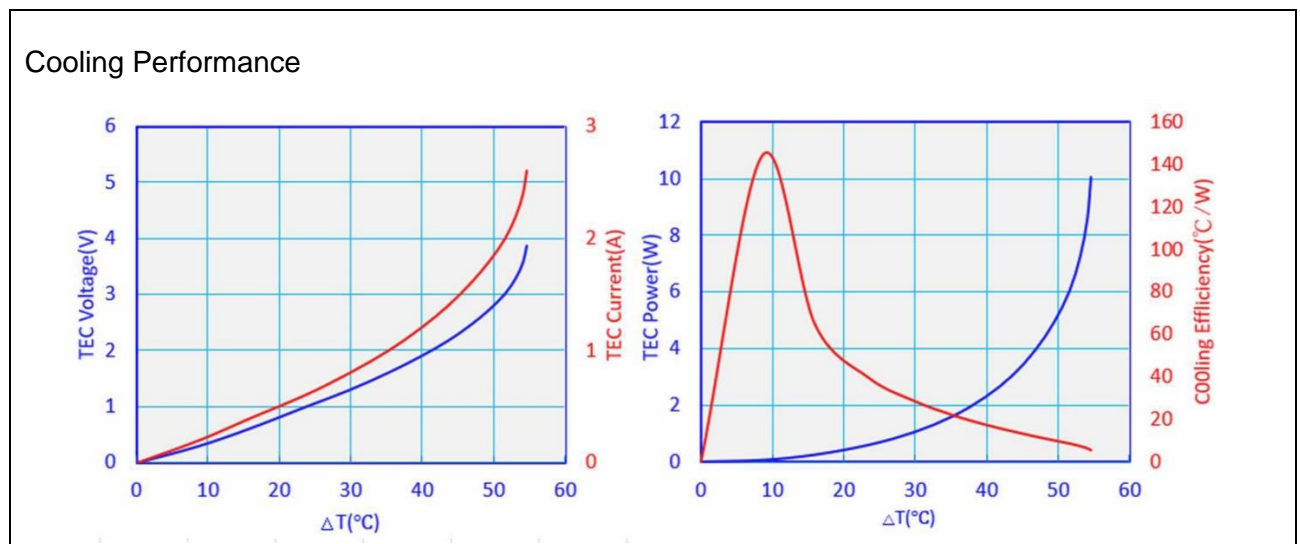
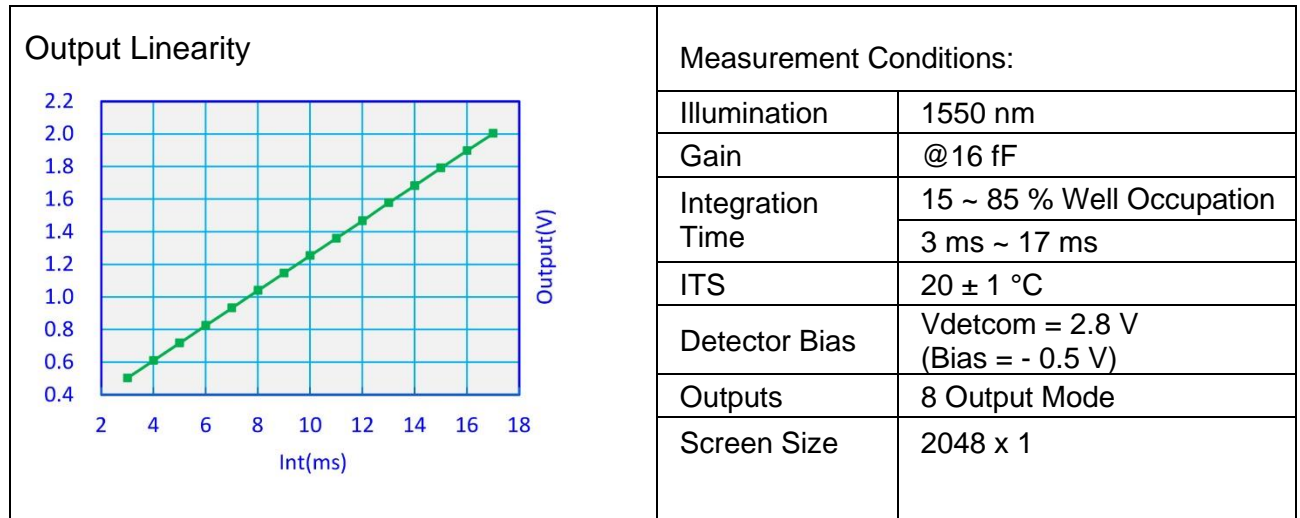
Pin #	Clocks	Levels	Rise / Fall	Remark
13	DATVALID	1.8 V / 0 V	--	Valid Data Output Flag Signal
22	SDOUT	1.8 V / 0 V	--	Data Code Output

### Analog Output

Pin #	Outputs	Levels	Value	Remark
9,26 10,25 11,24 12,23	VOUT_0, VOUT_1 VOUT_2, VOUT_3 VOUT_4, VOUT_5 VOUT_6, VOUT_7	0.2 ~ 2.4 V	--	Video Output
08	VTEMP	2.138 V	27 °C	Integrated Temperature Sensor (- 0.6 mV / °C)



## EXAMPLE CURVES



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