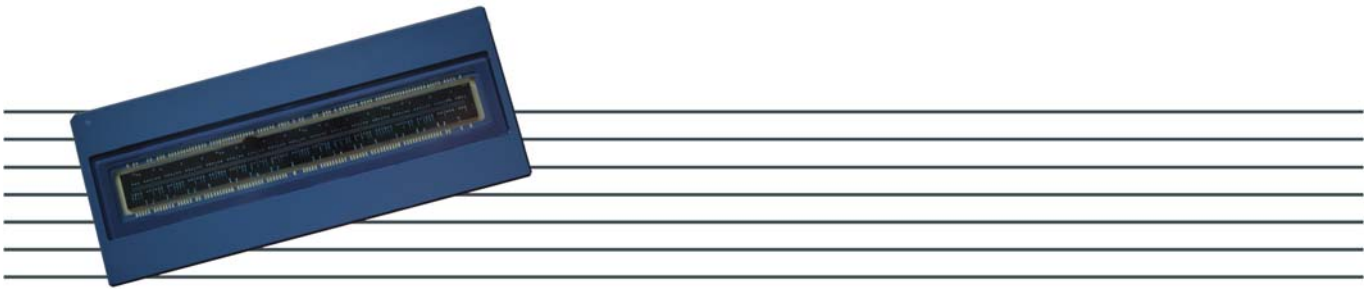


IT-FR-08192-00-R TDI CCD Image Sensor

Description:

With the IT-FR-08192-00-R sensor ANDANTA GmbH builds on and expands its line of proprietary TDI CCD image sensors by offering a low noise and high sensitivity sensor, particularly in near-infrared wavelengths while maintaining a high response in blue. The IT-FR sensor's superior performance makes it ideally suited for light-starved applications such as solar cell EL/PL inspection.

Features:

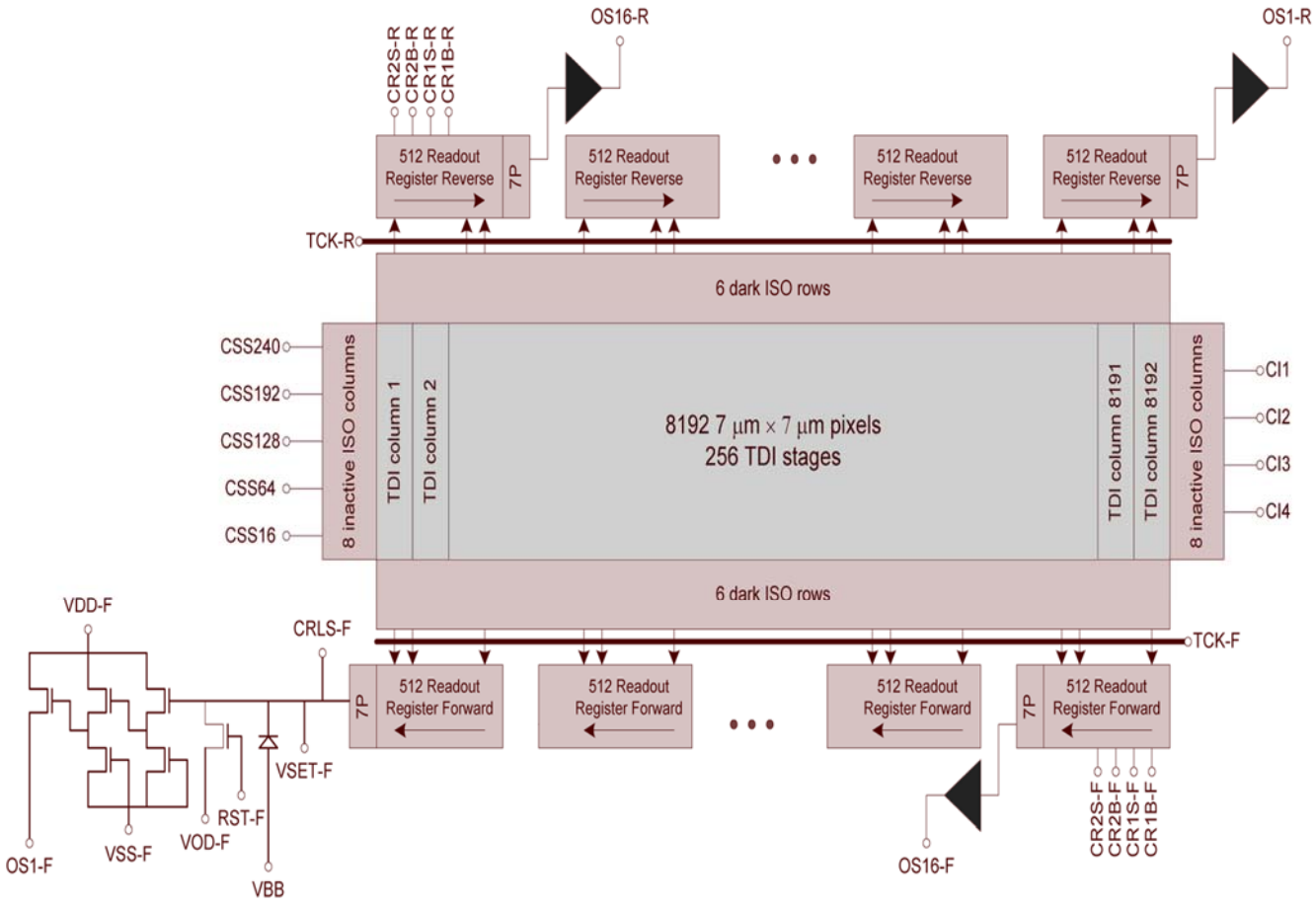
- Highly responsive, with a peak responsivity greater than 4,800 V/(µJ/cm^2) at 660 nm
- 16 taps, typical 20 MHz data rate[1] per tap
- TDI scan rate up to 34 KHz[1]
- 7 µm x 7 µm pixel size
- 8192 pixels
- Bi-directional TDI scan direction (forward / reverse selectable)
- 256 TDI stages (16, 64, 128, 192, 240, and 256 stages selectable)
- 100x lateral anti-blooming
- 2x horizontal binning on-chip[2]
- 1.3 W power consumption
- 162-pin ceramic PGA package
- ROHS compliant

Notes

[1]Contact ANDANTA GmbH for information concerning higher speed operations

[2]The sensor can accommodate 2x full well capacity in CRLS-x when horizontal binning is performed. Refer to Figure 5 for detailed timing of this operation

Functional Block Diagram:



Note

- Each side of the sensor has 8 inactive ISO columns that are not read out.
- There are also 6 dark ISO rows at the top and bottom of each frame.
- 7P represents 7 non-imaging pixels at the beginning of each line.

Table 1. Pin Functional Description:

Symbol	Function	Symbol	Function
VDD-x	Amplifier supply	CRxS-x	Readout register, storage phase
VSS-x	Amplifier ground	CRxB-x	Readout register, barrier phase
VBB	Substrate bias voltage	TCK-x	Transfer gate
VOD-x	Output reset drain	CIx	Image register, phase x
VSET-x	Set gate	CSSxxx	Stage selection gate
VLAB	Lateral anti-blooming bias voltage	OSx-x	Output signal
RST-x	Output reset gate	NC	No connection
CRLS-x	Readout register, last storage phase		

Table 2. Pinout

Package		Signal	Package Pin		Signal	Package Pin		Signal
A	1	OS15-R	B	1	VBB	C	1	OS16-R
	2	CRLS-R		2	VOD-R		2	VBB
	3	NC		3	VDD-R		3	OS14-R
	4	CR2B-R		4	TCK-R		4	VSET-R
	5	CR2S-R		5	VSS-R		5	OS13-R
	6	RST-R		6	CSS16		6	VOD-R
	7	CR1B-R		7	VBB		7	OS12-R
	8	CR1S-R		8	CSS64		8	VLAB
	9	CR2B-R		9	CSS128		9	OS11-R
	10	CR2S-R		10	CSS192		10	VDD-R
	11	RST-R		11	CRLS-R		11	OS10-R
	12	CR1B-R		12	NC		12	NC
	13	CR1S-R		13	CSS240		13	OS9-R
	14	CR2B-R		14	CRLS-R		14	VOD-R
	15	CR2S-R		15	NC		15	OS8-R
	16	RST-R		16	NC		16	VBB
	17	CR1B-R		17	NC		17	OS7-R
	18	CR1S-R		18	NC		18	VDD-R
	19	VSS-R		19	CSS16		19	OS6-R
	20	CR2B-R		20	CRLS-R		20	NC
	21	CR2S-R		21	NC		21	OS5-R
	22	RST-R		22	CSS64		22	VOD-R
	23	CR1B-R		23	CSS128		23	OS4-R
	24	CR1S-R		24	CSS192		24	VBB
	25	TCK-R		25	CSS240		25	OS3-R
	26	OS2-R		26	NC		26	NC
	27	NC		27	VLAB		27	OS1-R

Package		Signal	Package Pin		Signal	Package Pin		Signal
D	1	OS1-F	E	1	VLAB	F	1	NC
	2	VBB		2	VDD-F		2	OS2-F
	3	OS3-F		3	CI4		3	TCK-F
	4	VOD-F		4	CI3		4	CR2B-F
	5	OS4-F		5	CI1		5	CR2S-F
	6	CI2		6	CRLS-F		6	CR1B-F
	7	OS5-F		7	NC		7	CR1S-F
	8	NC		8	VBB		8	RST-F
	9	OS6-F		9	NC		9	CR2B-F
	10	NC		10	VSET-F		10	CR2S-F
	11	OS7-F		11	NC		11	CR1B-F
	12	VOD-F		12	CRLS-F		12	CR1S-F
	13	OS8-F		13	NC		13	RST-F
	14	NC		14	NC		14	CR2B-F
	15	OS9-F		15	NC		15	CR2S-F
	16	VBB		16	NC		16	CR1B-F
	17	OS10-F		17	CRLS-F		17	CR1S-F
	18	VSS-F		18	VSET-F		18	RST-F
	19	OS11-F		19	CI4		19	NC
	20	VOD-F		20	CI3		20	CR2B-F
	21	OS12-F		21	CI2		21	CR2S-F
	22	VBB		22	VDD-F		22	CR1B-F
	23	OS13-F		23	CI1		23	CR1S-F
	24	VLAB		24	TCK-F		24	RST-F
	25	OS14-F		25	VSS-F		25	CRLS-F
	26	VOD-F		26	NC		26	NC
	27	OS16-F		27	VBB		27	OS15-F

Functional Description

The IT-FR sensor is made up of the following three main functional groups:

1. A bidirectional 256-stage image shift register in which photogenerated charge packets are collected.
2. A CCD readout shift register.
3. A source-follower output amplifier that produces an output voltage.

Detection

The IT-FR image shift register is an array of 7 µm square pixels (aspect ratio 1:1) with a photosensitive area of 8192 μm^2 (90 % fill factor). The CI gates are not clocked during integration. Light incident on the pixels generates mobile charge carriers and the electrons are collected under the gates. The size of the accumulated charge packet depends linearly on the light intensity and the integration time. Immediately adjacent to the active pixels on both sides are 8 inactive pixels. Anti-blooming is achieved by biasing the lateral anti-blooming drain (VLAB) to a voltage to the recommended level so that only electrons beyond a certain packet size are drained away.

TDI Operation

Time-delay integration (TDI) line scan image sensors have very high responsivity that can be used to image objects that move rapidly in one dimension, even while using low-cost, low-maintenance and low-intensity light sources. The moving part that undergoes the scanning motion can be either the camera or the work-piece. For correct TDI operation, the sensor's line rate must be matched to the motion of the object relative to the sensor with the direction of motion parallel to the image register columns. In this way a charge packet corresponding to a particular region of the image tracks the object in the scene as the packet is transferred from line to line. In effect, each line of the final image is captured using 256 exposures, one per row of the image register. Both the integration time and the responsivity are 256 times greater than that of a comparable single-line array. For best results, mismatch between the TDI charge transfer and the object velocity should be less than 2 %.

Transfer

The image charge packets advance by a single line by clocking the CIx gates. The efficiency of each transfer is greater than 99.998 %. As part of the transfer sequence, one fully exposed line of the image is transferred in parallel from the light-shielded isolation rows to the readout shift register under the control of the transfer gate (TCK-x). The forward and reverse readout registers have separate transfer gates. The CR clocks must be stopped with CR1x-x high and CR2x-x low prior to the transfer. In both forward and reverse operations the signal charge is transferred from the CI4 phase of the image register to the CR1S phase of the readout register.

Output

A pseudo two-phase shift register is employed in the serial readout of charge packets by the output amplifier. The line of valid pixels is bracketed by 7 pre-scan pixels. The signal charge packets from the readout shift register are first transferred from the CR2x-x phase to CRLS-x, and then from CRLS-x over the set gate to the floating sense node diffusion. The potential due to the signal charge stored on this sense node capacitor serves as the voltage input to a low-noise 2.5-stage source-follower amplifier, resulting in an output voltage signal (OS-x). When the reset gate (RST-x) is pulsed to a high level, the sense node is cleared of charge to the voltage level of the output drain (VOD-x). After the node-reset operation, the sensor is ready to output the voltage signal due to the next signal charge packet in the shift register. To achieve two-fold horizontal binning, the CRLS-x clock frequency should be reduced to

50 % of the RST frequency. The OS pins require external load currents Iload. An active load is recommended for maximum gain and bandwidth. AC coupling is recommended to eliminate the DC offset. Note that the pre-scan pixels should not be used for calibration or detection.

Table 3. Absolute Maximum Ratings

Parameter	Unit	Min.	Max.
Storage Temperature	°C	-20	80
OperatingTemperature	°C	-20	60
Voltage on CRxS-x, CRxB-x, TCK-x, Clx, CSSxxx with respect to VBB	V	-20	20
Voltage on VDD-x, VSS-x, VOD-x, VSET-x, VLAB, RST-x, CRLS-x, OSxx-x with respect to VBB	V	0	20
I_{load}	mA	5	10

WARNINGS

1. Exceeding the listed values will void product warranty and may damage the sensor.
2. Electrostatic discharge (ESD) events and/or improper application of sensor biases can damage the sensor, and/or cause it to not function within the realms of specification compliance. Proper sensor power on/off sequence provided in Table 4 should be followed to prevent damage to the sensor.

CAUTION! These devices are sensitive to damage from electrostatic discharge (ESD). The leads should be shorted together during storage or handling to prevent damage to the device.

Table 4. Safe and Proper Functioning

Requirement	Implementation
ESD	Observe standard ESD procedures.
Clocks and biases for ESD-protected pins	RST and CRLS pins, having on-chip ESD protection structures, should not be clocked nor biased to negative voltages (reference to VBB).
Power-ON sequence	1. Clear all voltages to 0 V prior to sensor insertion 2. Set VBB 3. Set VSS 4. Set RST 5. Set VOD 6. Set VDD 7. Set VLAB 8. Set rest of voltages in any order
Power-OFF sequence	Reverse order of the ON sequence.

Table 5. Input / Output Characteristics

Input characteristics: capacitance per pin to VBB[1]	Units	Typical
CRxx-x	pF	157
CRLS-x	pF	31
RST-x	pF	34
TCK-x	pF	291
CSSxxx	pF	448
Clx	nF	8
Output characteristics[2]	**Units**	**Typical**
Output Impedance	Ω	125
DC output offset	V	9.5

Notes

[1]Measured using 1 MHz signal with DC bias of 1 V and AC amplitude of 100 mV.
[2]With I_{load} = 5 mA.

Table 6. DC Operating Conditions

Symbol	Units	Min.	Rec.	Max.
VDD-x	V	16	18	18
VSS-x	V	—	0	—
VBB[1]	V	—	-2	—
VOD-x	V	14	16	16
VSET-x	V	1.5	2.5	2.5
VLAB	V	13	14	15
I_{load}	mA	5	5	10

Notes

1. When deviating from the recommended biases, ensure that the new biases still meet the essential conditions in Table 8.
2. VBB should never be forward biased with respect to VSS.

WARNING: To prevent damage to the sensor, a Schottky diode must connect VBB and VSS.

Table 7. AC Operating Conditions

Symbol		Units	Min.	Rec.	Max.
RST-x	Low Swing	V	5.0 9.0	5.5 9.5	6.0 10.0
CRLS-x	Low Swing	V	-2.0	-1.5 5.0	-1.0
CRxS-x	Low Swing	V	-1.5	-1.0 5.0	-0.5
CRxB-x	Low Swing	V	-7.5	-7.0 5.0	-6.5
TCK-x	Low Swing	V	-7.5 9.5	-7.0 10.0	-6.5 10.5
Clx	Low Swing	V	-7.5 9.5	-7.0 10.0	-6.5 10.5
CSSxxx	Enabled Disabled	V	-11.5	-11.0 Same as Clx	-10.5

Notes

When deviating from the recommended biases, ensure that the new biases still meet the essential conditions in Table 8.

Table 8. Essential Bias Conditions

Conditions	If condition not satisfied, the sensor will exhibit
VLAB with respect to Clx < 24 V	Non-uniformity in full well vertically across the imaging area.

Table 9. Performance Specifications

Specification	Unit	Min.	Typ.	Max.
Saturation output voltage (VSAT)	mV	720	840	880
Full well capacity (FWC)	Electrons	40,000	46,000	48,000
Charge conversion efficiency (CCE)	μV/electrons	18	18.4	
RMS noise	mV rms		0.54	
Wavelength of peak responsivity			660	
Peak responsivity	V/(μJ/cm²)	4,800	4810	
Dynamic range	dB		64	
Noise equivalent exposure (NEE)	pJ/cm²		0.11	
Saturation equivalent exposure (SEE)	nJ/cm²		0.18	
Fixed pattern noise (FPN)[5]	mV		2	6
Photoresponse non-uniformity (PRNU)[5]	% OS		2.5	15
Charge transfer efficiency (CTE) Image register Readout register		 0.99998 0.99999		
Dark signal[6]	mV		0.16	

Test Conditions

1. Data rate = 20 MHz.
2. Line rate = 34 KHz.
3. Operating temperature = 30 °C.
4. Tungsten halogen light source, black body temperature of 3200 K, filtered with 750 nm IR cut-off filter.
5. Measured with full stages.
6. See Figure 3 for typical dark current density measured at various temperatures.

Figure 2. Typical Responsivity and Quantum Efficiency

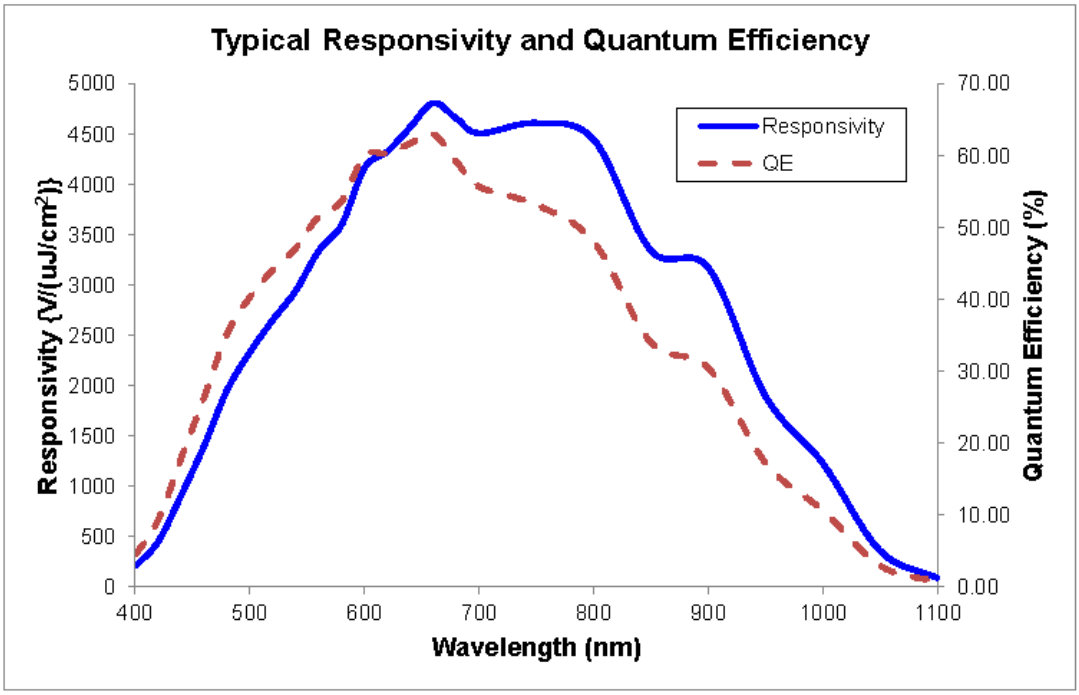
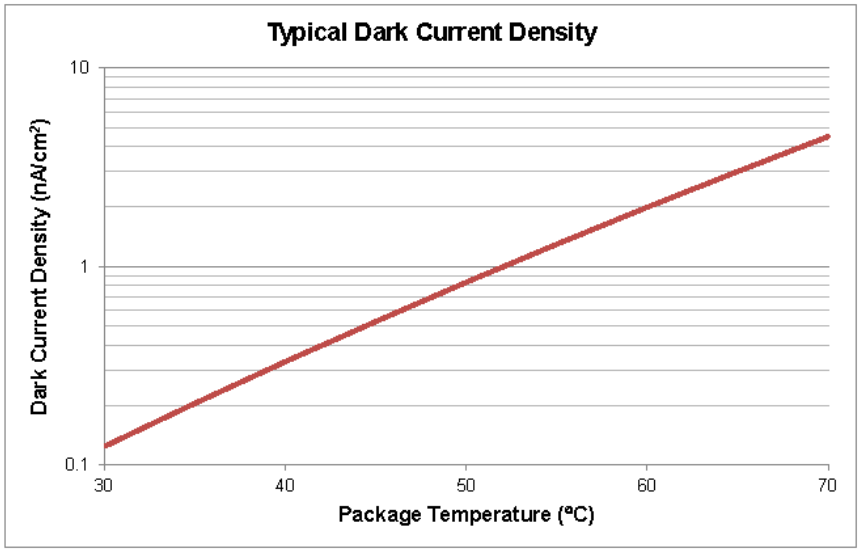


Figure 3. Typical Dark Current Density



Note
The package temperature is the temperature measured on the back surface of the sensor package during normal operation at temperature = 30 °C.

Table 10. Timing Parameters

Time	Description	Units	Value
t1	Vertical transfer duration	ns	1600
t2	Vertical transfer to horizontal transfer	ns	> 50
t3	RST-x width	ns	10
t4	Data period	ns	50
t5	CRLS-x period for x2 horizontal binning	ns	100

Figure 4. Overall Timing

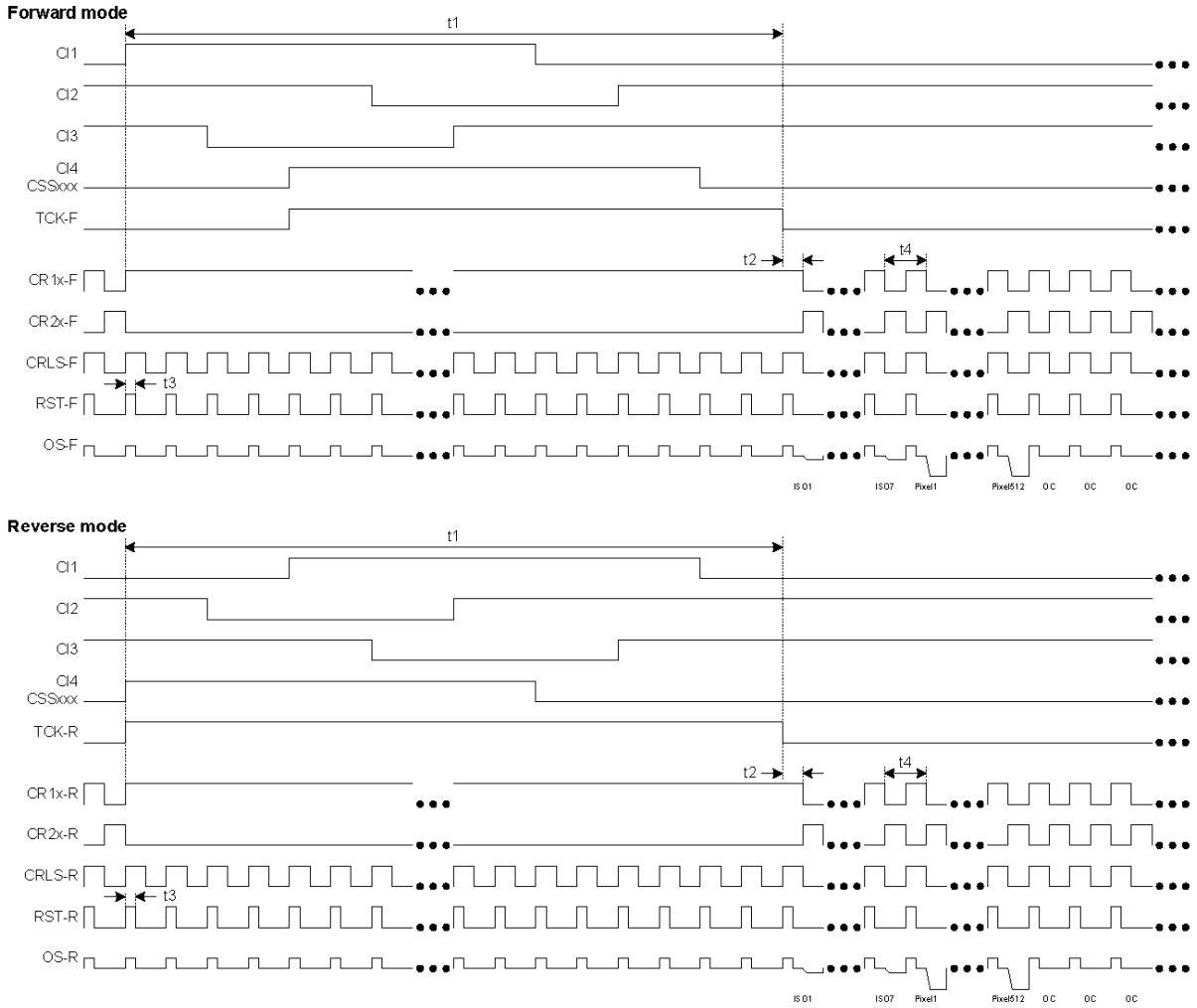
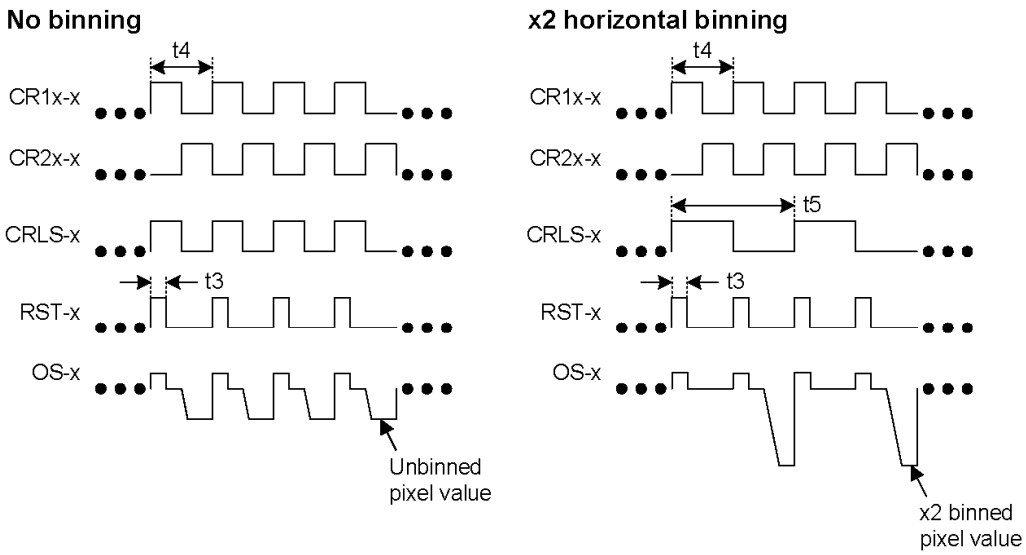


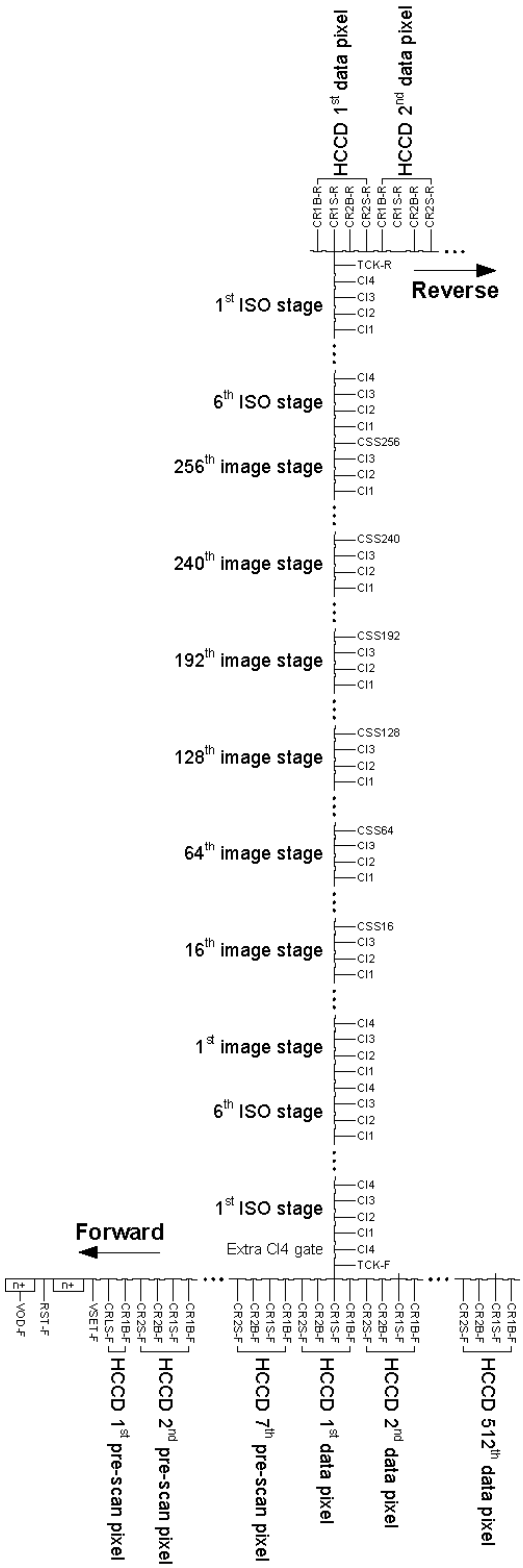
Figure 5. Detailed Readout Register Timing: no binning vs. ×2 horizontal binning



Notes

1. CRLS-x is the same phase as CR1S-x when binning is not performed.
2. To achieve 2x horizontal binning, the CRLS-x clock frequency should be reduced to 50 % of the RST frequency.

Figure 6. Gate Structure Diagram



Notes

1. Charge transfers over TCK-x into CR1S-x.
2. CSSxxx gates replace CI4 gates.

Figure 7. Package Dimensions