



FPA320x256-C

NEAR INFRARED (0.9 μm - 1.7 μm)

320x256 InGaAs Focal Plane Array

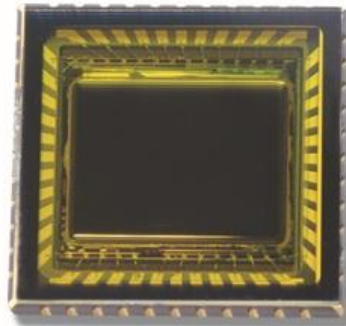
FEATURES

- 320 x 256 Array Format
- 0.9 μm – 1.7 μm Spectral Range
- Light Weight 44CLCC Package
- Minimum Pixel Operability > 99.9 %
- Quantum Efficiency > 70 %
- Room Temperature Operation
- Built-in Temperature Sensor
- Snapshot ITR¹/IWR² and IMRO³ Readout Modes
- 1, 2 or 4 Outputs with up to 10 MHz Pixel Rate
- Windowing Capability

APPLICATIONS

- Near-infrared Imaging
- Covert Surveillance
- Semiconductor/Solar Panel Inspection
- Medical Science and Biology
- Fiberoptic Assembly and Testing
- See through Fog/Smoke
- Ice/Slush/Moisture Mapping
- Industrial Thermal Imaging
- Astronomy and scientific
- Sorting and recycling

¹ITR: Integrate-Then-Read - ²IWR: Integrate-While-Read - ³IMRO: Integration with Multiple ReadOut



GENERAL DESCRIPTIONS

PARAMETER	UNIT	VALUE
Sensor Technology	--	Planar InGaAs PIN
Spectral Range	μm	0.9 – 1.7
Actual Pixel Array	--	320 x 256
Effective Pixel Array	--	318 x 254
Pixel Pitch	μm	30
Image Size	mm	9.6 x 7.68
Package Type	--	44-pin Ceramic LCC
Package Size L x W x T	mm	16.510 x 16.510 x 2.456
Weight	g	1.6



SPECIFICATIONS ($T_{AMB} = 22^{\circ}C$)

PARAMETER		UNIT	TYPICAL VALUE	COMMENTS
Dark Current ^{1,2}		fA	≤ 200	Photopixel Biased @ -0.5 V
Quantum Efficiency * Fill Factor (QE _{EFF}) ^{1,2}		%	≥ 70	$\lambda = 1.0 \mu m - 1.6 \mu m$
Response Nonuniformity ^{1,2}		%	≤ 10	At 50 % Full Well
Response Nonlinearity ^{1,2}		%	≤ 2	15 % - 85 % Well Occupation Range
Charge Capacity	@ High Gain 13.3 $\mu V/e^-$	Me ⁻	0.17	ROIC Specifications
	@ Low Gain 0.7 $\mu V/e^-$		3.50	
Readout Noise		e ⁻ _{RMS}	≤ 70	ROIC Specifications High Gain, Tint = 16 msec
Output Swing		V	2.8	
Minimum Integration Period ²		μs	5.5	Assuming 5 MHz Master Clock
Pixel Operability ^{1,2}		%	MIN. VALUE	Percentage of Pixels with QE _{EFF} Deviation within $\pm 20\%$ (QE _{EFF} Mean)
			≥ 99.9	

1. These items are defined for central effective pixel array (318x254). Their values correspond to default operation conditions.
2. Contact us for further information.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	UNIT	MIN.	MAX.
Operation Temperature ³	$^{\circ}C$	-40	+71
Storage Temperature ³	$^{\circ}C$	-40	+71
Power Consumption	mW	--	175

3. In non-condensing environment.



OPERATING CONDITIONS

Bias Input

Pin #	Bias	Voltage	Current	Remark
06	VPD	5.5 V	< 1 mA	Logic positive supply
07	VND	0 V	< 1 mA	Logic negative supply
23	VPOSOUT	5.5 V	< 25 mA	Output stage analog supply
17	VNEGOUT	0 V	< 25 mA	Output stage analog ground
30	VPOS	5.5 V	< 5 mA	Positive analog supply
29	VNEG	0 V	< 15 mA	Negative analog supply and substrate
40	VPOS_CORE	5.5 V	< 15 mA	CTIA amplifier positive supply
39	VDETCOM	4.7 V - 5.5 V	< 5 mA	Detector common voltage Detector bias = VDETCOM-4.7*

4. VDETCOM lower than 4.7V will forward bias the sensor, the exact zero bias voltage is device and temperature dependent.

Digital Pattern Input

Pin #	Clocks	Levels	Rise/Fall	Remark
05	CLK	0 V - 5.5 V	< 10 ns	Master clock Max. Freq.=5 MHz
03	FSYNC	0 V - 5.5 V	< 10 ns	Frame sync - controls frame start and integration time
04	LSYNC	0 V - 5.5 V	< 10 ns	Line sync - controls line readout timing
02	DATA	0 V - 5.5 V	< 10 ns	Data code input - programs device function registers in Control Mode Left open in Default Mode

Clocks	Synchronization
FSYNC	Rising and falling when CLK is rising
LSYNC	Rising and falling when CLK is falling
DATA	Rising and falling when CLK is rising



Analog Video Output

Pin #	Outputs	Levels	Settle	Remark
18	OUTA	1.3 V to 4.2 V	< 50 ns to 0.1 %	Output A used in single output mode
19	OUTB	1.3 V to 4.2 V	< 50 ns to 0.1 %	Output A and B used in two output mode
20	OUTC	1.3 V to 4.2 V	< 50 ns to 0.1 %	Output A, B, C, and D used in four output mode
21	OUTD	1.3 V to 4.2 V	< 50 ns to 0.1 %	Output A, B, C, and D used in four output mode
22	OUTR	3 V	-	Reference for common mode output

Gain & Bandwidth Selection in Default Mode

Pin #	Functions	Low	High	Remark
01	GAIN	0 V C = 10 fF	5.5 V C = 210 fF	Selects unit cell integration capacitor, Left open in Control Mode
44	BWL	0 V Low BW	5.5 V High BW	Selects bandwidth limiting capacitor in unit cell, Left open in Control Mode

Advanced Function

Pin #	Functions	Voltages	Remark
27	VCAS ⁵	3.75 V	CTIA amplifier cascode FET bias
26	VOUTREF ⁵	3 V	Output reference level during blanking period
25	VBLM ⁵	2 V	Detector bloom control
28	IMSTR_ADJ ⁶	0 V - 5.5 V	Adjusts analog master bias current
24	VOS	0 V - 5.5 V	Variable Offset/Skimming Control Voltage
41	TEMP	0 V - 5.5 V	On chip temperature monitor 0.74V at 300K, Slope = -14.8 mV/10K in 50-300 K
43	VTESTIN	1.5 V - 4.5 V	For use in IC function test Left open in FPA operation
42	TESTOUT	0 V - 5.5 V	

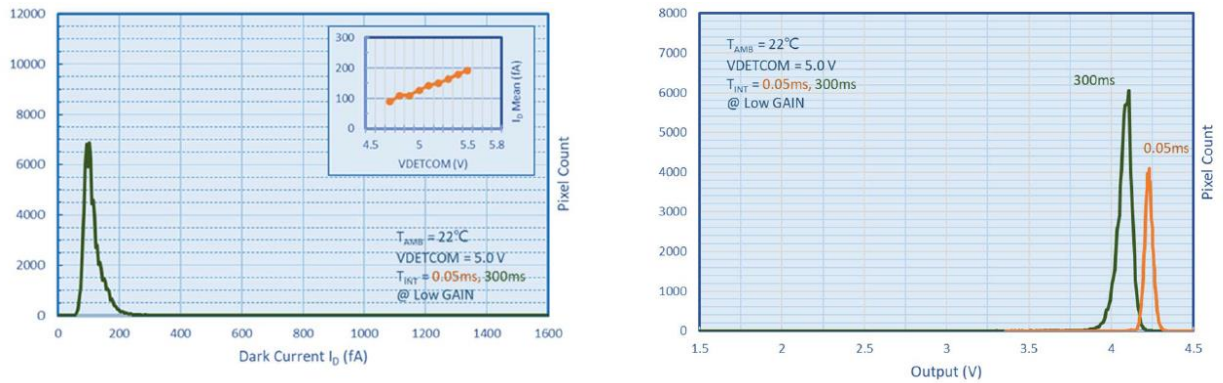
5. Internally generated after bias input, but can be overridden.

6. Also addressable through control register (DATA).

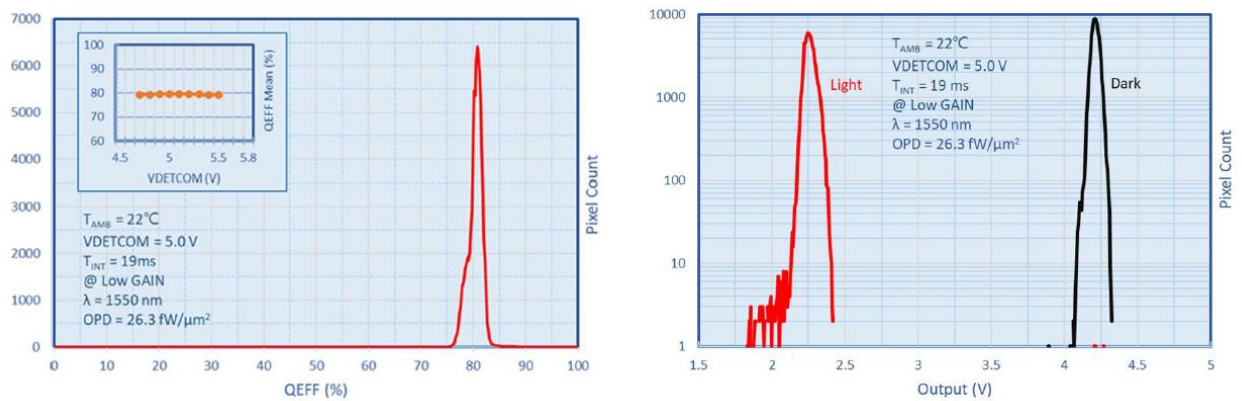


EXAMPLE CURVES

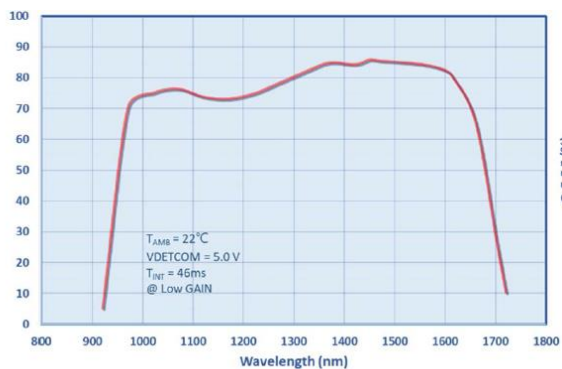
Histograms of Dark Condition



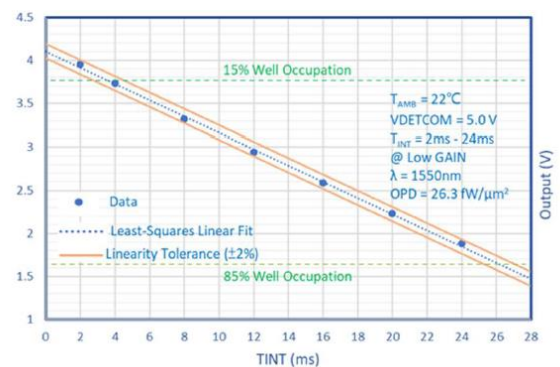
Histograms of Illumination Condition



QE FF Spectrum

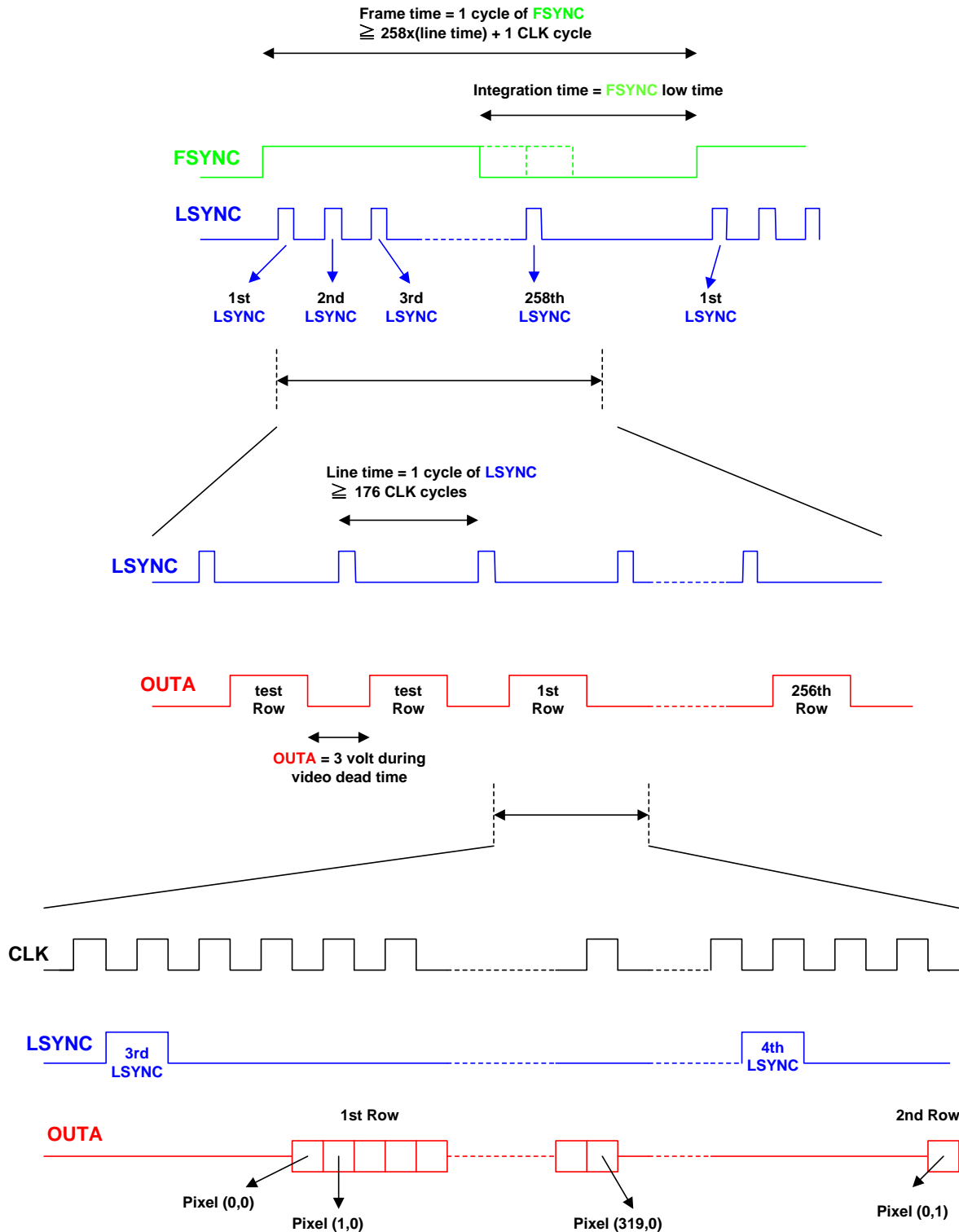


Output Linearity



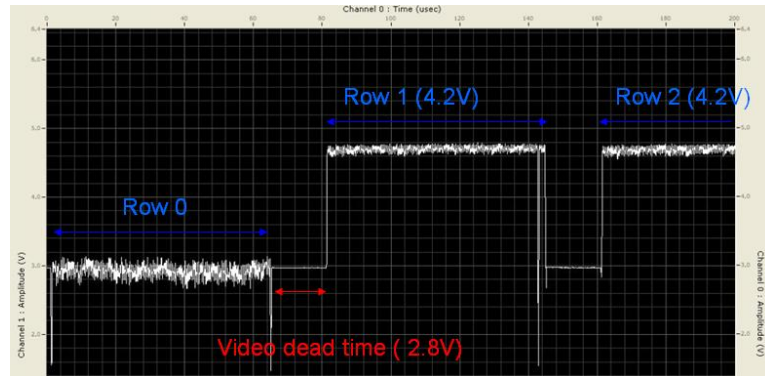


TIMING CHART FOR DEFAULT MODE OPERATION

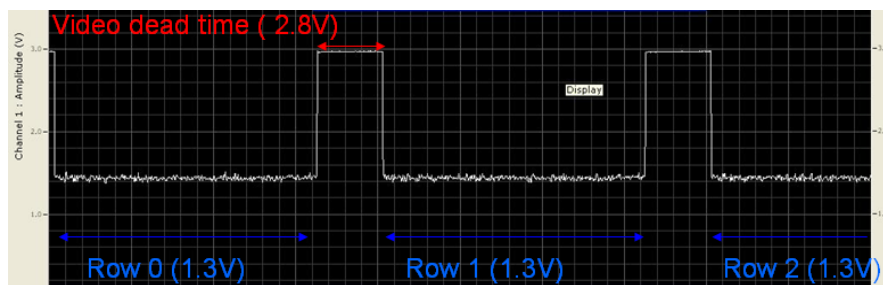




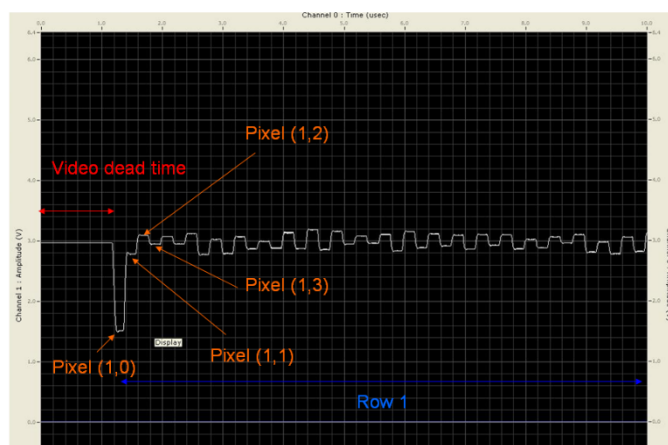
OUTA waveform under dark



OUTA waveform under saturation



OUTA waveform under half saturation



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