



FPA-320x256-K-2.2-TE2 InGaAs Imager

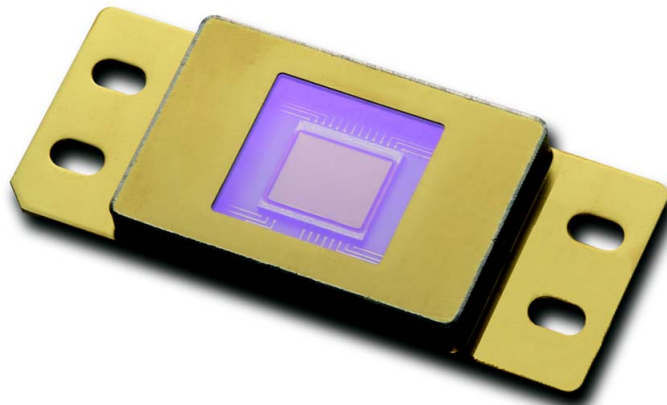
NEAR INFRARED (1.2 μm - 2.2 μm) IMAGE SENSOR

FEATURES

- 320 x 256 Array Format
- 28-pin Metal DIP Package
- Embedded 2-stage Thermoelectric Cooler
- Typical Pixel Operability > 98 %
- Quantum Efficiency > 70 %
- Low dark current

APPLICATIONS

- Near-infrared Imaging
- Imaging Spectroscopy
- Covert Surveillance
- Nondestructive Inspection
- Medical Science and Biology
- Astronomy and Scientific
- Industrial Thermal Imaging
- Moisture Mapping



GENERAL DESCRIPTIONS

PARAMETER	VALUE
Sensor Technology	In _{0.73} Ga _{0.27} As/InP
Spectral Range	1.2 μm - 2.2 μm
Image Format	320 (H) x 256 (V)
Pixel Pitch	30 μm x 30 μm (> 99 % Fill Factor)
Image Size	9.6 mm (H) x 7.68 mm (V)
Package Type	28-pin Metal DIP Package
Weight	25.6 g (TBR)



FPA CHARACTERISTICS ($T_a = 253 \text{ K}$)

PARAMETER	TYPICAL	CONDITIONS
Dark Current	$\leq 10 \text{ pA}$	Pixel bias = 0.1 volt
Quantum Efficiency	$\geq 70 \%$	$\lambda = 1.4 \text{ } \mu\text{m} - 2.1 \text{ } \mu\text{m}$
Fill Factor	$> 99 \%$	
Detectivity	$\geq 1 \times 10^{12} \text{ Jones}$	$T_{\text{int}} = 1 \text{ ms}$, Low Gain, $\lambda = 2 \text{ } \mu\text{m}$
Response Nonuniformity	$\leq 40 \%$	Under 50 % Saturation
Nonlinearity (Max. Deviation)	$\leq 2 \%$	Over 20 % - 80 % Full Well Capacity
Max. Pixel Rate	10 MHz	
Gain	High: $13.3 \text{ } \mu\text{V/e}^-$ Low: $0.7 \text{ } \mu\text{V/e}^-$	
Full Well	High: 170 K e^- Low: 3.5 M e^-	
Pixel Operability*	$> 97 \%$ (Minimum)	Dark Current $\leq 25 \%$ Full Well Response Nonuniformity $\leq 40 \%$

* Pixel Operability is defined within the center 318 x 254 regions

ABSOLUTE MAXIMUM RATINGS

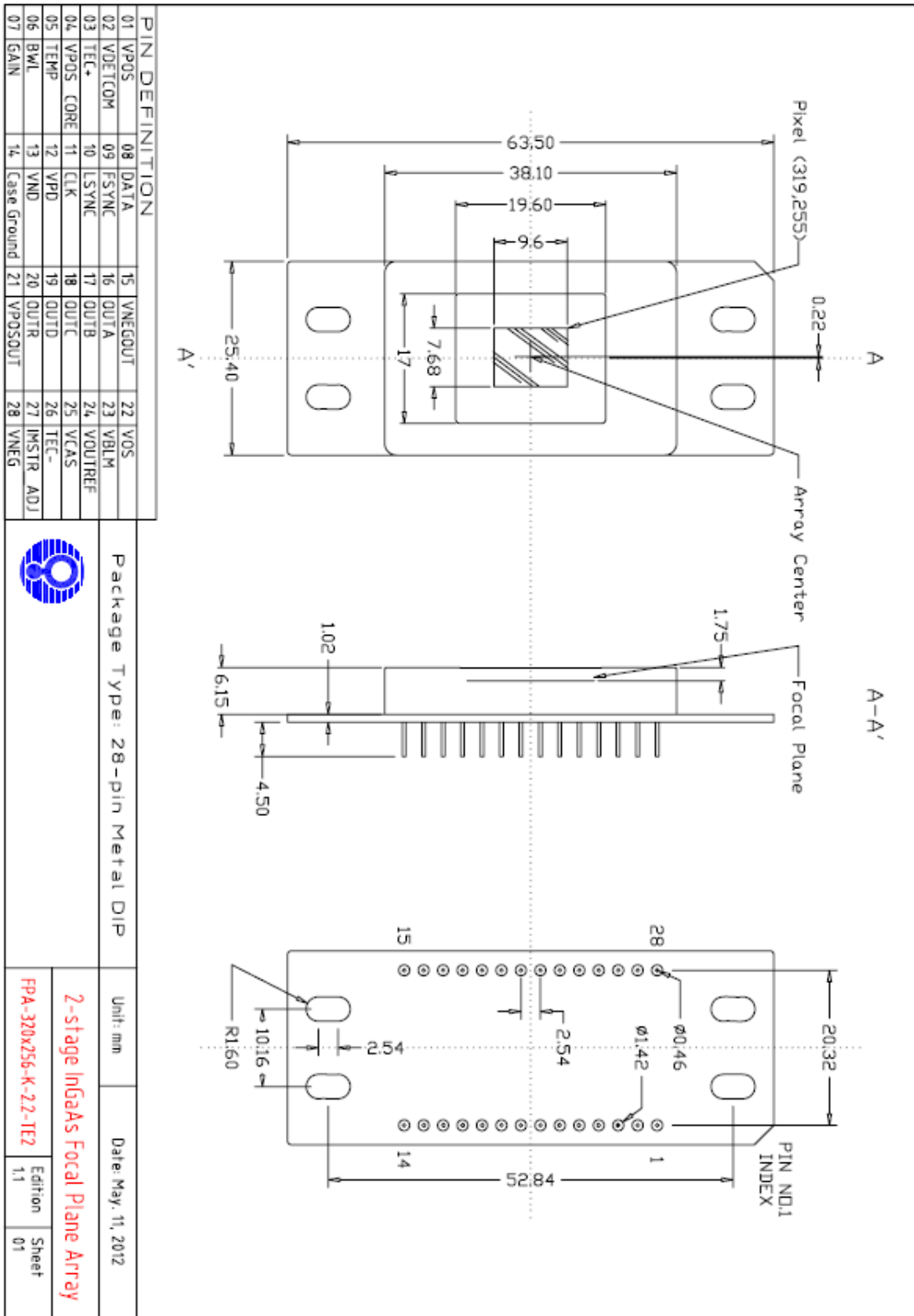
PARAMETER	UNIT	MIN	MAX
Operation Temperature*	$^{\circ}\text{C}$	- 40	85
Storage Temperature*	$^{\circ}\text{C}$	- 40	85
Power Consumption	mW	---	175 **

* Denotes environment temperature, not chip temperature

** Without driving the cooler



PACKAGE OUTLINE



Note : ID number of the imager is printed on the flank of the package



OPERATING CONDITIONS

Bias Input

Pin #	Bias	Voltage	Current	Remark
12	VPD	5.5 V	< 1 mA	Logic positive supply
13	VND	0 V	< 1 mA	Logic negative supply
21	VPOSOUT	5.5 V	< 25 mA	Output stage analog supply
15	VNEGOUT	0 V	< 25 mA	Output stage analog ground
1	VPOS	5.5 V	< 5 mA	Positive analog supply
28	VNEG	0 V	< 15 mA	Negative analog supply and substrate
4	VPOS_CORE	5.5 V	< 15 mA	CTIA amplifier positive supply
2	VDETCOM	4.4 V - 5.5 V	< 5 mA	Detector common voltage Detector bias = VDETCOM - 4.4*

* VDETCOM lower than 4.4V will forward bias the sensor at 253K, the zero bias voltage is device and temperature dependent, please refer individual sensor test reports

Digital Pattern Input

Pin #	Clocks	Levels	Rise/Fall	Remark
11	CLK	0 V - 5.5 V	< 10 ns	Master clock Max. Freq. = 5 MHz
9	FSYNC	0 V - 5.5 V	< 10 ns	Frame sync - controls frame start and integration time
10	LSYNC	0 V - 5.5 V	< 10 ns	Line sync - controls line readout timing
8	DATA	0 V - 5.5 V	< 10 ns	Data code input - programs device function registers in Control Mode Left open in Default Mode

Clocks	Synchronization
FSYNC	Rising and falling when CLK is rising
LSYNC	Rising and falling when CLK is falling
DATA	Rising and falling when CLK is rising



Video Output

Pin #	Outputs	Levels	Settle	Remark
16	OUTA	1.3 V to 4.2 V	< 50 ns to 0.1 %	Output A used in single output mode
17	OUTB	1.3 V to 4.2 V	< 50 ns to 0.1 %	Output A and B used in two output mode
18	OUTC	1.3 V to 4.2 V	< 50 ns to 0.1 %	Output A, B, C, and D used in four output mode
19	OUTD	1.3 V to 4.2 V	< 50 ns to 0.1 %	Output A, B, C, and D used in four output mode
20	OUTR	3 V	-	Reference for common mode output

Gain & Bandwidth Selection in Default Mode

Pin #	Functions	Low	High	Remark
7	GAIN	0 V C = 10 fF	5.5 V C = 210 fF	Selects unit cell integration capacitor Left open in Control Mode
6	BWL	0 V Low BW	5.5 V High BW	Selects bandwidth limiting capacitor in unit cell Left open in Control Mode

Advanced Function

Pin #	Functions	Voltages	Remark
25	VCAS*	3.75 V	CTIA amplifier cascode FET bias
24	VOUREF*	3 V	Output reference level during blanking period
23	VBLM*	2 V	Detector bloom control
27	IMSTR_ADJ**	0 V - 5.5 V	Adjusts analog master bias current
22	VOS	0 V - 5.5 V	Variable Offset/Skimming Control Voltage
5	TEMP***	0 V - 5.5 V	On chip temperature monitor ~0.74 V at 300 K, Slope = -14.8 mV / 10 K in 50 – 300 K

* Internally generated after bias input, but can be overridden.

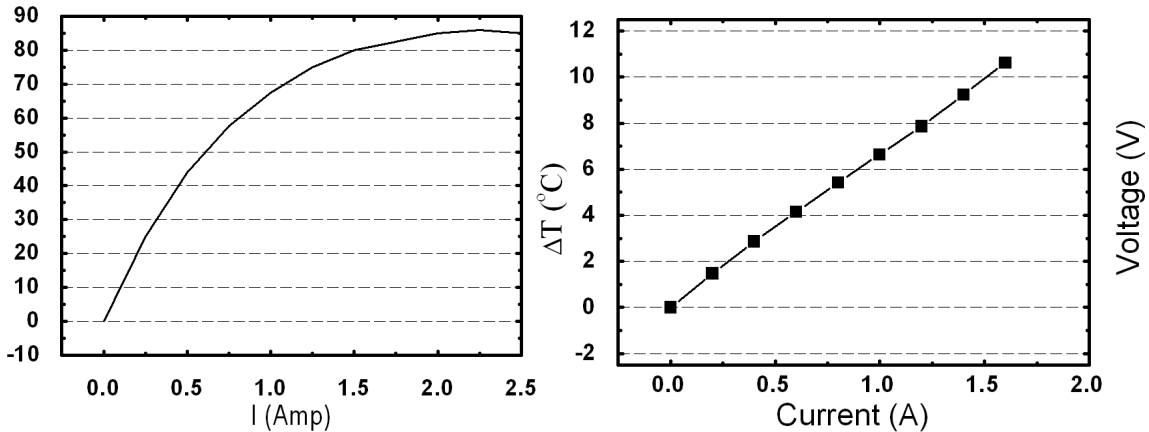
** Also addressable through control register (DATA).

*** The intersection voltage at 300K varies among sensors, but the slope is unchanged.

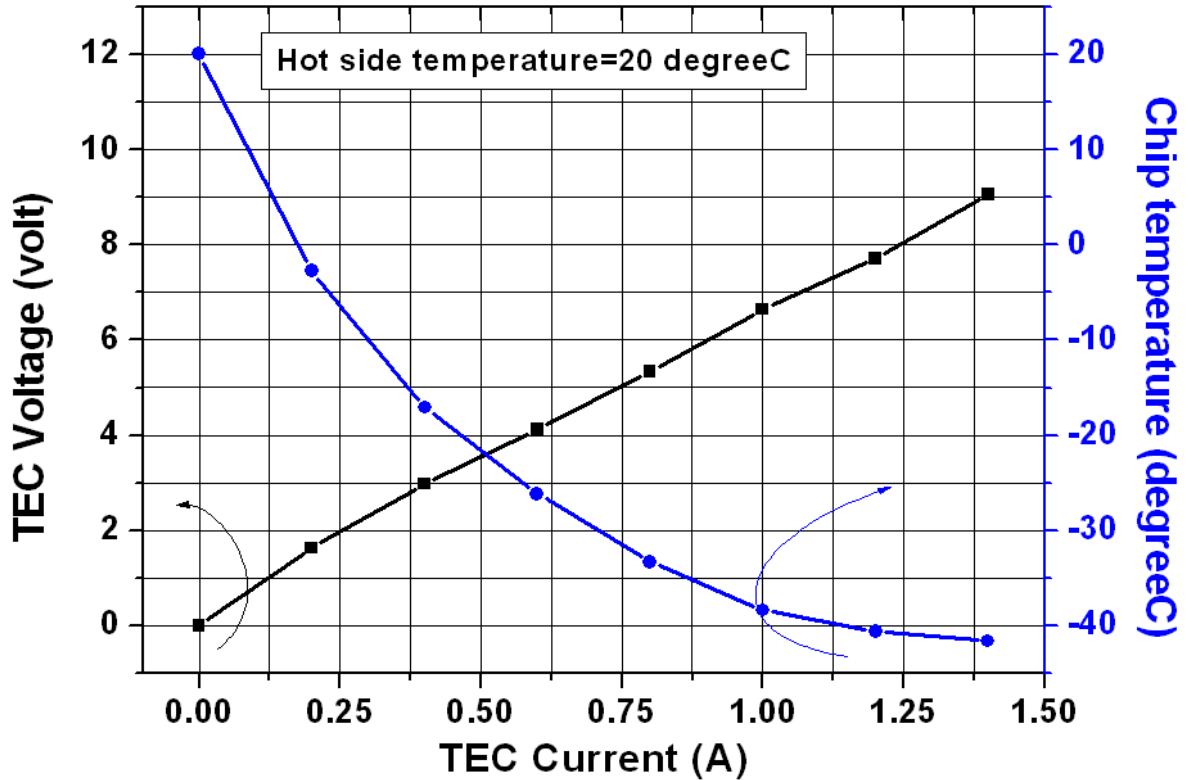


THERMOELECTRIC COOLER DATA (Without thermal loading)

ΔT_{\max}	I_{\max}	V_{\max}
91 °C	2.4 A	11.7 V

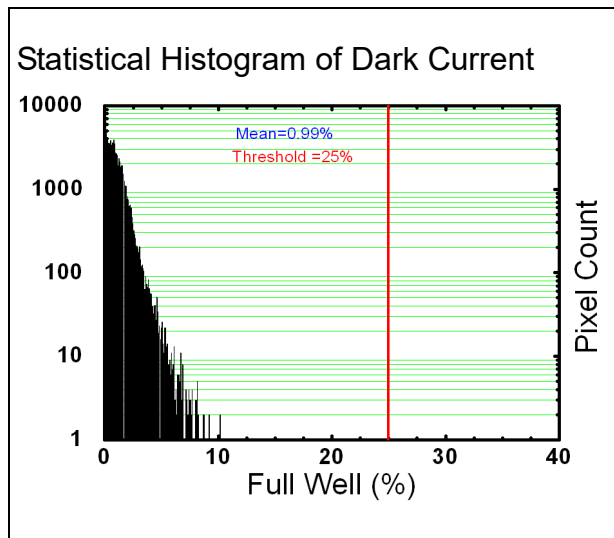


Cooling Performance with sensor loading and operating

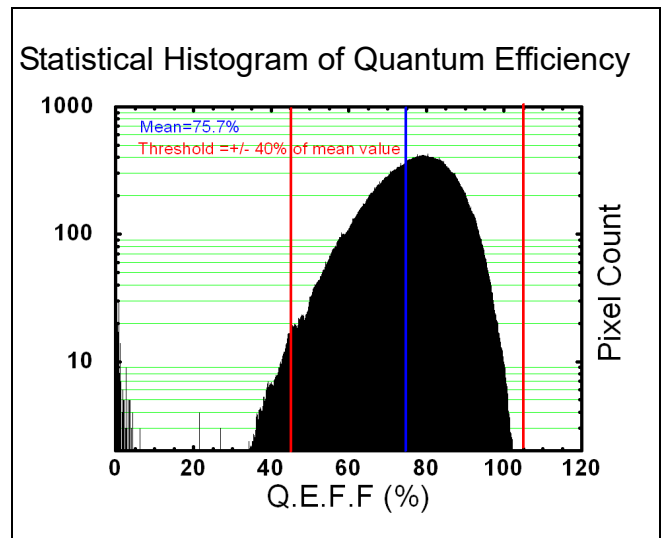




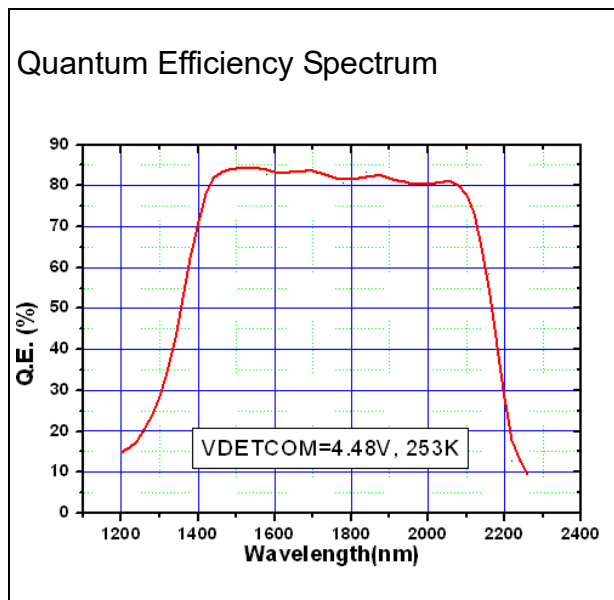
EXAMPLE CURVES



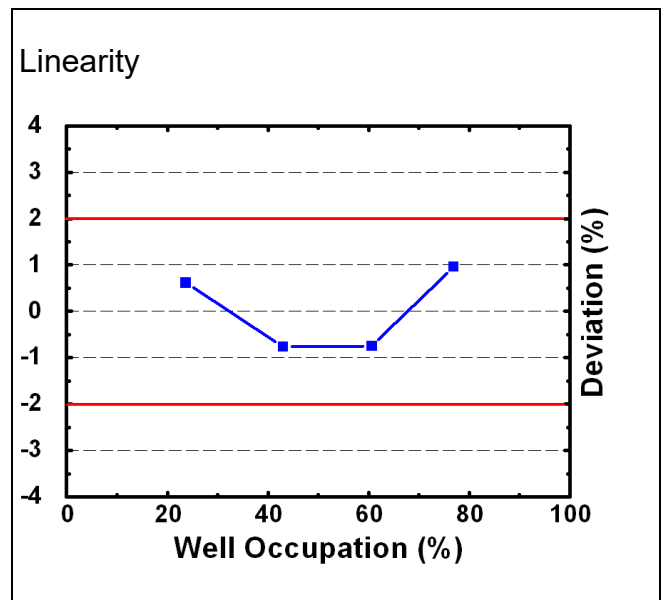
Test Conditions:	
Illumination	Dark
Wavelength	---
Gain	Low
Integration Time	1 ms
Remark	Effective Screen



Test Conditions:	
Illumination	Nonuniformity $\leq \pm 0.15\%$
Wavelength	2000 nm
Gain	Low
Integration Time	2.4 msec, 50 % saturation
Remark	Effective Screen



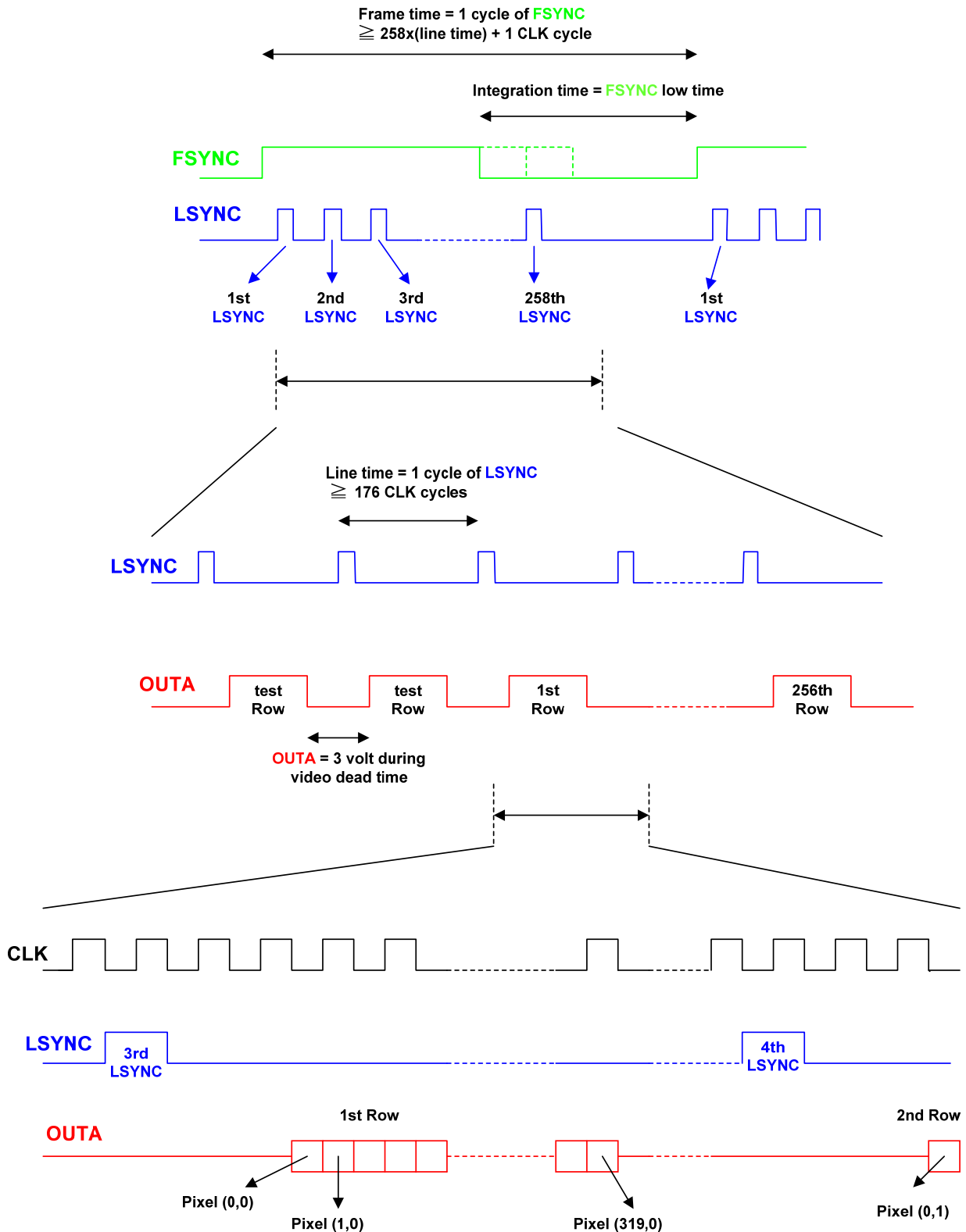
Test Conditions:	
Illumination	Nonuniformity $\leq \pm 0.15\%$
Wavelength	Broadband
Gain	Low
Integration Time	2.4 ms, 50 % saturation
Remark	Effective Screen Array Average



Test Conditions:	
Illumination	Nonuniformity $\leq \pm 0.15\%$
Wavelength	2000nm
Gain	Low
Integration Time	1 ms, 2 ms, 3 ms, 4 ms
Remark	Effective Screen Array Average

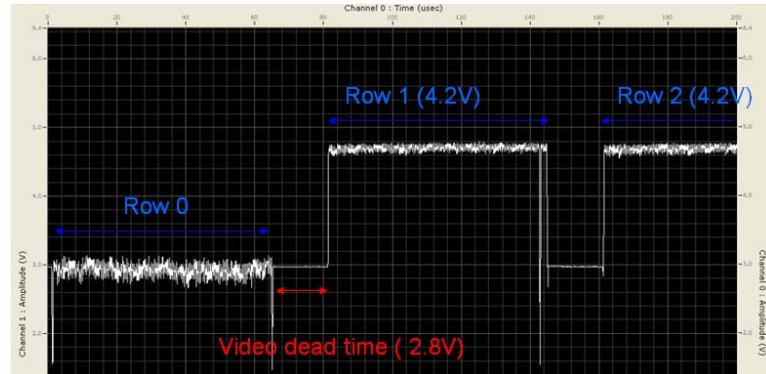


TIMING CHART FOR DEFAULT MODE OPERATION

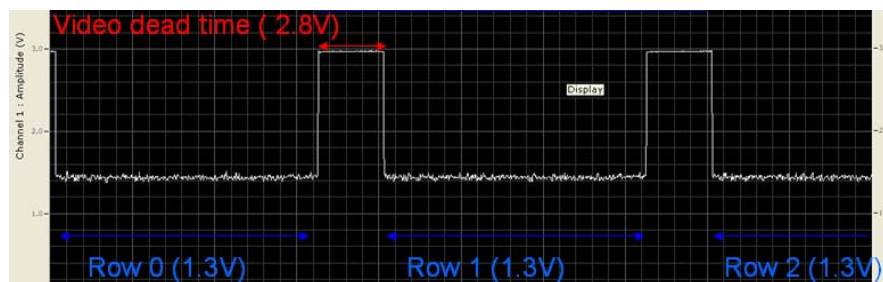




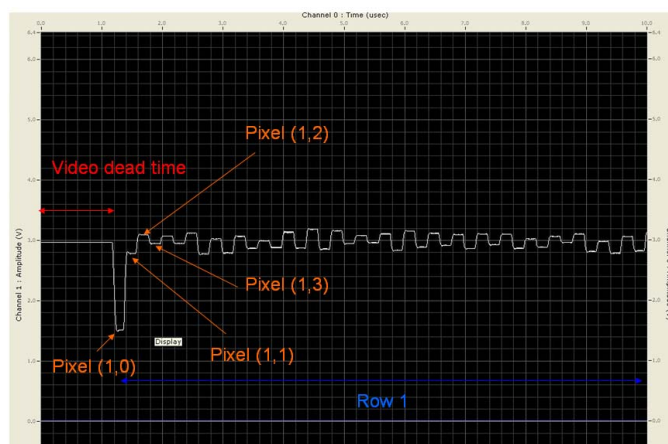
OUTA waveform under dark



OUTA waveform under saturation



OUTA waveform under half saturation



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