



FPA320x256-1.9-TS2-50mm

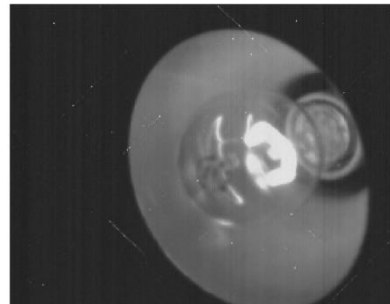
Near-Infrared (1.1 μm - 1.9 μm) InGaAs Focal Plane Array

FEATURES

- 320 x 256 Array Format
- 28-pin Metal DIP Package
- Embedded Thermoelectric Cooler
- Built-in Temperature Sensor
- 1.1 μm - 1.9 μm Spectral Range
- Minimum Pixel Operability > 99%
- Quantum Efficiency > 70 %
- Snapshot ITR / IWR and IMRO Readout Modes
- 1, 2 or 4 Outputs with up to 10 MHz Pixel Rate
- Windowing Capability

APPLICATIONS

- Shortwave-Infrared Imaging
- Hyper- / Multi-Spectral Imaging
- Semiconductor Inspection / Process Monitoring
- Medical Science and Biology
- Fiberoptic Assembly and Testing
- See through Fog / Smoke
- Ice / Slush / Moisture Mapping
- Laser Beam Profiling
- Astronomy and Scientific
- Sorting, Recycling



Halogen lamp
(Unretouched image)
Low GAIN
mode Int. 1ms
@ -40°C

GENERAL DESCRIPTIONS

PARAMETER	UNIT	VALUE
Sensor Technology	--	Planar InGaAs PIN
Spectral Range	μm	1.1 - 1.9
Actual Pixel Array	--	320 x 256
Effective Pixel Array	--	318 x 254
Pixel Pitch	μm	30
Image Size	mm	9.6 x 7.68
Package Type	--	28-pin Metal DIP Package
Package Size L x W x T	mm	50.0 x 25.4 x 11.67
Weight	g	27.5



SPECIFICATIONS (ITS¹ = 40°C)

PARAMETER		UNIT	TYPICAL VALUE	COMMENTS
Dark Current ^{2,3}		fA	≤ 300	Photopixel Biased @ 0 V
Quantum Efficiency * Fill Factor (QE _{EFF}) ²		%	≥ 70	λ = 1700 nm
Response Nonuniformity ²		%	≤ 10	At 50 % Full Well
Response Nonlinearity ²		%	≤ 4	15 % - 85 % Well Occupation Range
Charge Capacity	@ High Gain, 13.3 μV/ e ⁻	Me ⁻	0.17	ROIC Specifications
	@ Low Gain, 0.7 μV/ e ⁻		3.50	
Readout Noise		e ⁻ _{RMS}	< 70	ROIC Specifications
Output Swing		V	2.7	
Minimum Integration Period		μs	5.5	Assuming 5MHz Master Clock
Pixel Operability ²		%	Min. Value	Percentage of Pixels with QE _{EFF} Deviation within ± 20 % (QE _{EFF} Mean)
			≥ 99	

1. Readings from Integrated Temperature Sensor (ITS).
2. These items are defined for central effective pixel array (318x254). Their values correspond to default operation conditions.
3. Low Gain, T_{int} = 300ms – 100ms.

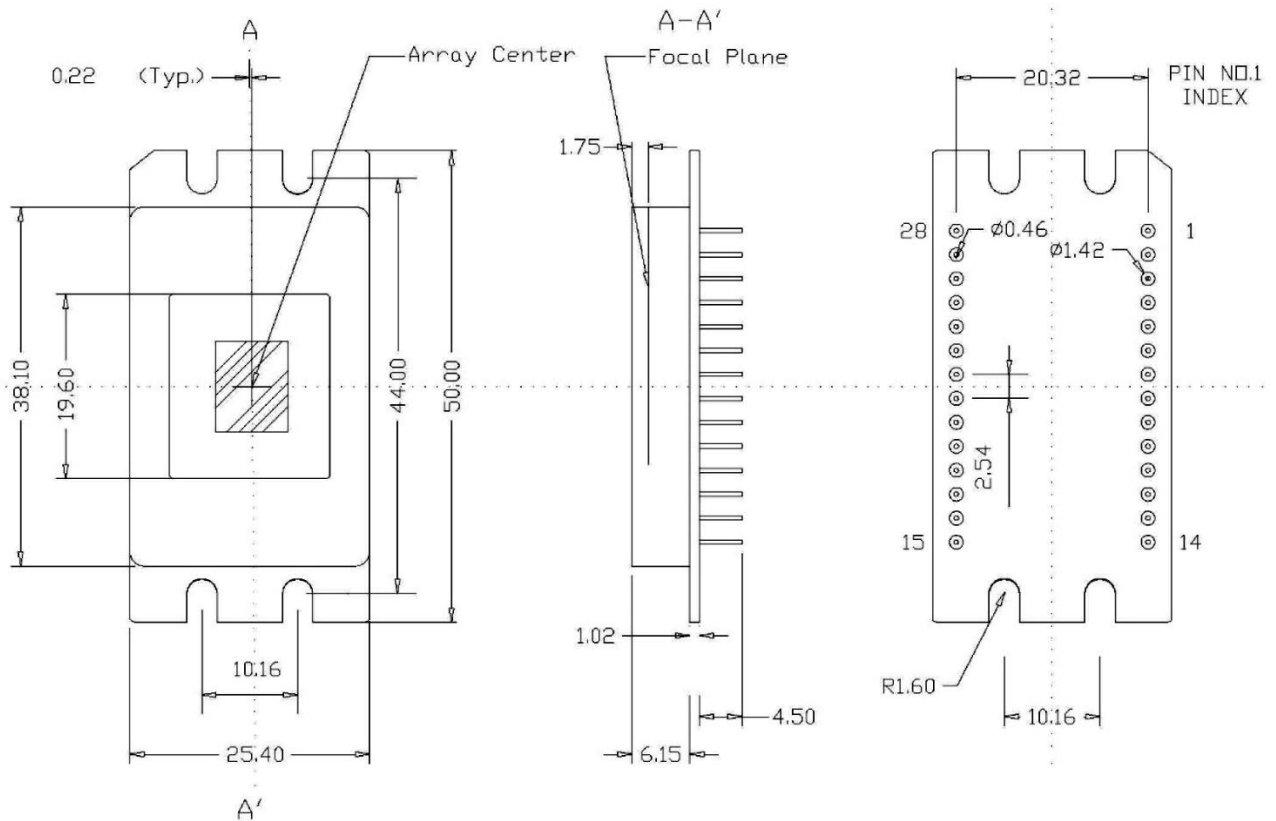
ABSOLUTE MAXIMUM RATINGS

PARAMETER	UNIT	MIN.	MAX.
Operation Temperature ⁴	°C	-40	+71
Storage Temperature ⁴	°C	-40	+71
Power Consumption ⁵	mW	--	175
TEC Bias ⁶	V	--	4.8
TEC Current ⁶	A	--	1.8

4. Non-condensing environment.
5. Without powering on the thermoelectric cooler.
6. Applied to Pin-3 for cooling operation. Operation above these maximum ratings causes excessive (local) heat accumulation and may result in permanent damage to the cooler.



PACKAGE OUTLINE (Unit: mm)



Note: ID Number of the imager is printed on the flank of the package.

PIN DEFINITION							
01	VPOS	08	DATA	15	VNEGOUT	22	VOS
02	VDETCOM	09	FSYNC	16	OUTA	23	VBLM
03	TEC+	10	LSYNC	17	OUTB	24	VOUTREF
04	VPOS_CORE	11	CLK	18	OUTC	25	VCAS
05	TEMP	12	VPD	19	OUTD	26	TEC-
06	BWL	13	VND	20	OUTR	27	IMSTR ADJ
07	GAIN	14	CASE GROUND	21	VPOSOUT	28	VNEG



OPERATING CONDITIONS

Bias Input

Pin #	Bias	Voltage	Current	Remark
12	VPD	5.5 V	< 1 mA	Logic positive supply
13	VND	0 V	< 1 mA	Logic negative supply
21	VPOSOUT	5.5 V	< 25 mA	Output stage analog supply
15	VNEGOUT	0 V	< 25 mA	Output stage analog ground
01	VPOS	5.5 V	< 5 mA	Positive analog supply
28	VNEG	0 V	< 15 mA	Negative analog supply and substrate
04	VPOS_CORE	5.5 V	< 15 mA	CTIA amplifier positive supply
02	VDETCOM	4.5 V - 5.5 V	< 5 mA	Detector common voltage Detector bias ^{6a} = VDETCOM-4.5

6a. VDETCOM lower than 4.5 V will forward bias the sensor, the exact zero bias voltage is device and temperature dependent, please refer to the individual sensor test report.

Digital Pattern Input

Pin #	Clocks	Levels	Rise/Fall	Remark
11	CLK	0 V - 5.5 V	< 10 ns	Master clock, Max. Freq. = 5 MHz
09	FSYNC	0 V - 5.5 V	< 10 ns	Frame sync - controls frame start and integration time
10	LSYNC	0 V - 5.5 V	< 10 ns	Line sync - controls line readout timing
08	DATA	0 V - 5.5 V	< 10 ns	Data code input – programs device function registers in Control Mode. Left open in Default Mode

Clocks	Synchronization
FSYNC	Rising and falling when CLK is rising
LSYNC	Rising and falling when CLK is falling
DATA	Rising and falling when CLK is rising



Analog Video Output

Pin #	Outputs	Levels	Settle	Remark
16	OUTA	1.3V to 4.2V	< 50ns to 0.1%	Output A used in single output mode
17	OUTB	1.3V to 4.2V	< 50ns to 0.1%	Output A and B used in two output mode
18	OUTC	1.3V to 4.2V	< 50ns to 0.1%	Output A, B, C, and D used in four output mode
19	OUTD	1.3V to 4.2V	< 50ns to 0.1%	Output A, B, C, and D used in four output mode
20	OUTR	3 V	---	Reference for common mode output

Gain & Bandwidth Selection in Default Mode

Pin #	Functions	Low	High	Remark
07	GAIN	0V C=10fF	5.5V C=210fF	Selects unit cell integration capacitor Left open in Control Mode
06	BWL	0V Low BW	5.5V High BW	Selects bandwidth limiting capacitor in unit cell Left open in Control Mode

Advanced Function

Pin #	Functions	Voltages	Remark
25	VCAS ⁷	3.75V	CTIA amplifier cascode FET bias
24	VOUREF ⁷	3V	Output reference level during blanking period
23	VBLM ⁷	2V	Detector bloom control
27	IMSTR_ADJ ⁸	0V - 5.5V	Adjusts analog master bias current
22	VOS	0V - 5.5V	Variable Offset/Skimming Control Voltage
05	TEMP ⁹	0V - 5.5V	On chip temperature monitor 0.74V at 300K, Slope=-14.8mV/10K in 50 – 300K

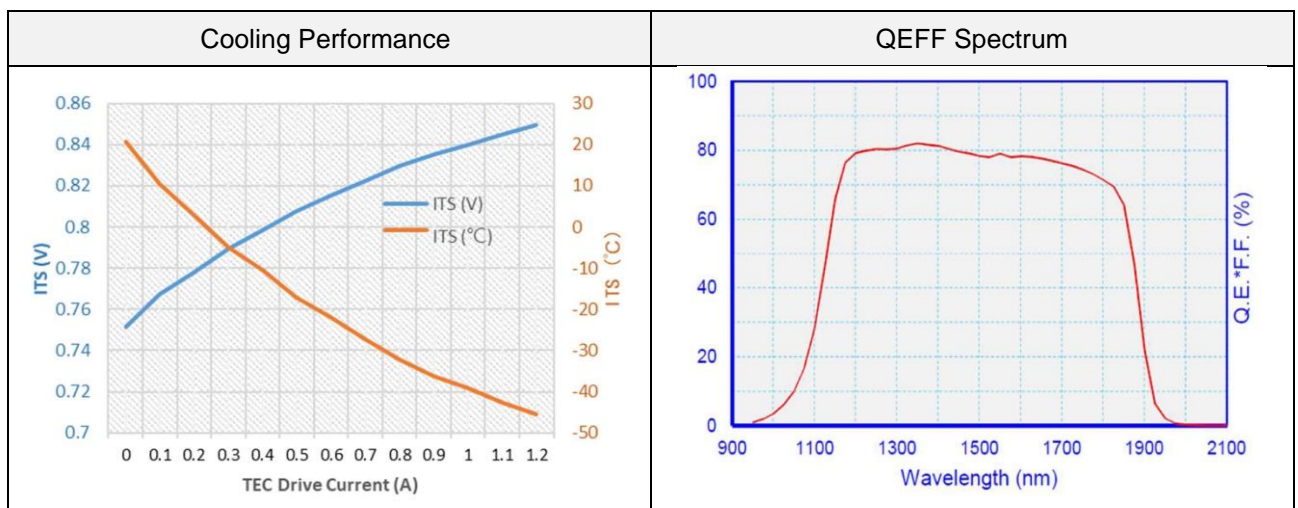
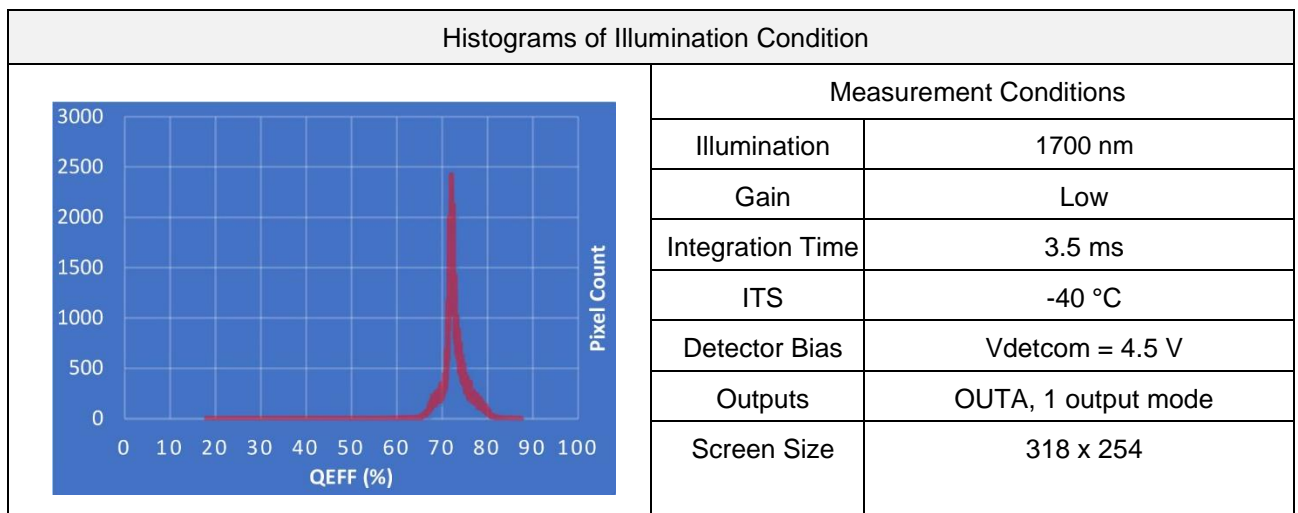
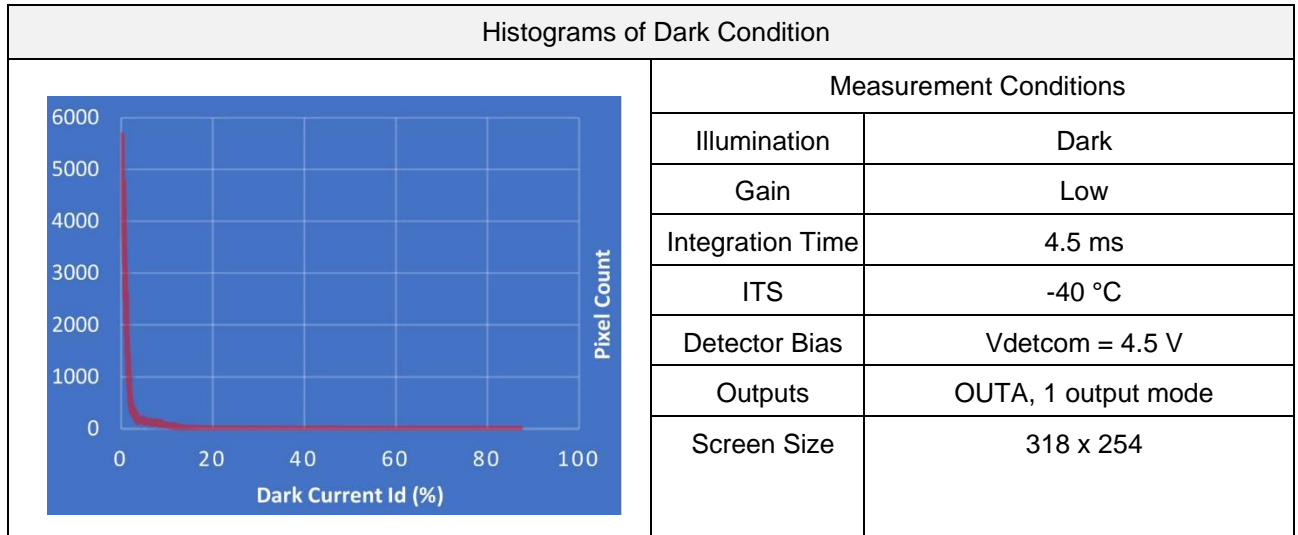
7. Internally generated after bias input but can be overridden.

8. Also addressable through control register (DATA).

9. The intersection voltage at 300K varies among sensors, but the slope is unchanged.

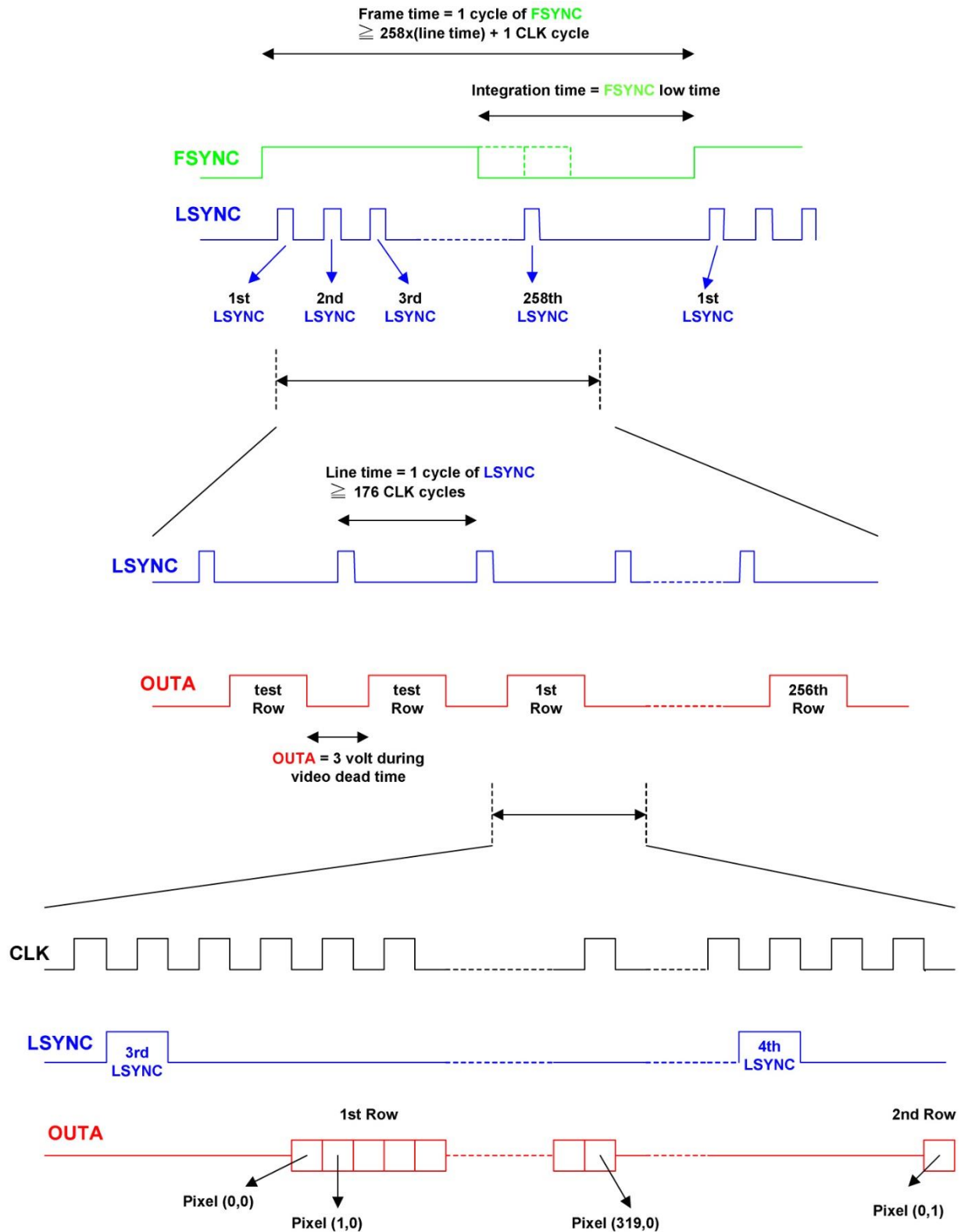


EXAMPLE CURVES



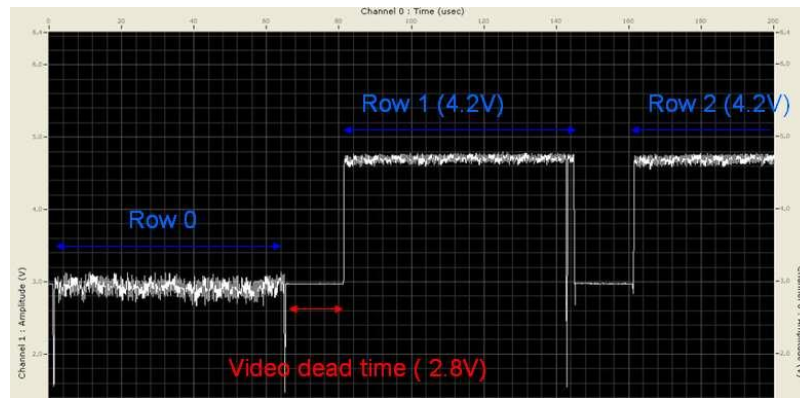


TIMING CHART FOR DEFAULT MODE OPERATION

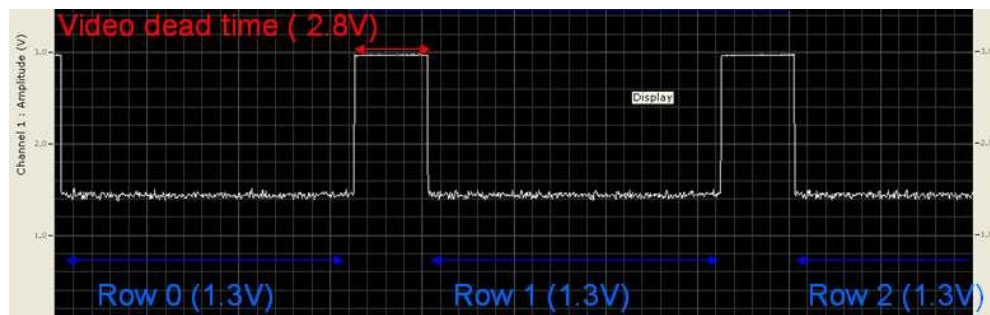




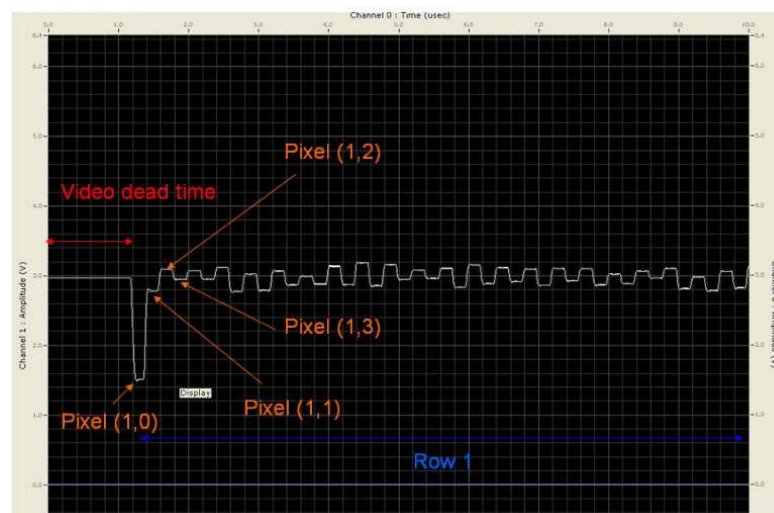
OUTA Waveform under dark



OUTA Waveform under saturation



OUTA Waveform under half saturation



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