



# FPA-320x256-C InGaAs Imager

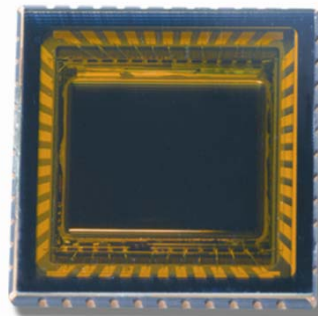
## NEAR INFRARED (0.9 $\mu\text{m}$ - 1.7 $\mu\text{m}$ ) IMAGE SENSOR

### FEATURES

- 320 x 256 Array Format
- Light Weight 44CLCC Package
- Hermetic Sealed Glass Lid
- Typical Pixel Operability > 99.5 %
- Quantum Efficiency > 70 %
- Room temperature operation

### APPLICATIONS

- Near-infrared Imaging
- Imaging Spectroscopy
- Covert Surveillance
- Semiconductor Inspection
- Medical Science and Biology
- Fiberoptic Telecommunication
- Astronomy and Scientific
- Industrial Thermal Imaging
- Moisture Mapping



### GENERAL DESCRIPTIONS

PARAMETER	VALUE
Sensor Technology	Standard InGaAs/InP
Spectral Range	0.9 $\mu\text{m}$ - 1.7 $\mu\text{m}$
Image Format	320 (H) x 256 (V)
Pixel Size	30 $\mu\text{m}$ x 30 $\mu\text{m}$ (> 99 % Fill Factor)
Image Size	9.6 mm (H) x 7.68 mm (V)
Package Type	44-pin Ceramic LCC
Weight	1.6 g



## FPA CHARACTERISTICS ( $T_a = 25^\circ\text{C}$ )

PARAMETER	TYPICAL	CONDITIONS
Dark Current	< 0.4 pA	0.1 Volt detector bias
Quantum Efficiency	$\geq 70 \%$	$\lambda = 1.0 \mu\text{m} - 1.6 \mu\text{m}$
Fill Factor	> 99 %	
Adjacent pixel crosstalk	< 1%	
Detectivity	$\geq 5 \times 10^{12}$ Jones	$T_{\text{int}} = 16 \text{ ms}$ , High Gain, $\lambda = 1.55 \mu\text{m}$
Response Nonuniformity	$\leq 10 \%$	Under 50% Saturation
Nonlinearity (Max. Deviation)	$\leq 2 \%$	10 % - 90 % Full Well Capacity
Max. Pixel Rate	10 MHz	
Gain	High gain: 13.3 $\mu\text{V}/e^-$ Low gain: 0.7 $\mu\text{V}/e^-$	
Full Well	High gain: 170 K $e^-$ Low gain: 3.5 M $e^-$	
Pixel Operability*	> 99 % (Minimum)	Dark Current $\leq 20 \%$ Full Well Response Nonuniformity $\leq 20 \%$

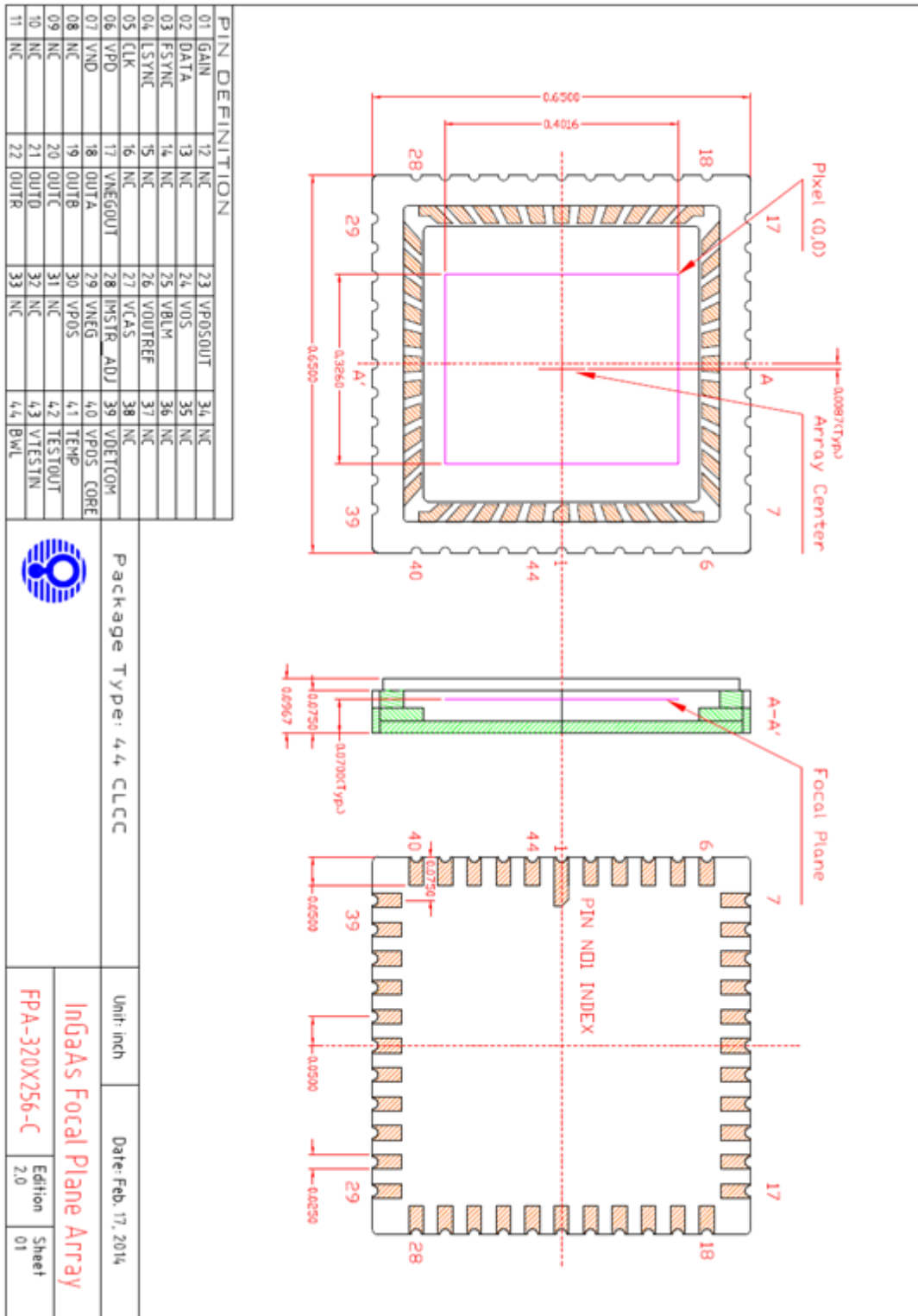
\* Pixel Operability is defined within the center 318 x 254 regions

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	UNIT	MIN	MAX
Operation Temperature	$^\circ\text{C}$	- 20	85
Storage Temperature	$^\circ\text{C}$	- 40	85
Power Consumption	mW	---	175



## PACKAGE OUTLINE



Note : ID number of the imager is printed on the backside of the package



## OPERATING CONDITIONS

### Bias Input

Pin #	Bias	Voltage	Current	Remark
6	VPD	5.5 V	< 1 mA	Logic positive supply
7	VND	0 V	< 1 mA	Logic negative supply
23	VPOSOUT	5.5 V	< 25 mA	Output stage analog supply
17	VNEGOUT	0 V	< 25 mA	Output stage analog ground
30	VPOS	5.5 V	< 5 mA	Positive analog supply
29	VNEG	0 V	< 15 mA	Negative analog supply and substrate
40	VPOS_CORE	5.5 V	< 15 mA	CTIA amplifier positive supply
39	VDETCOM	4.7 V - 5.5 V	< 5 mA	Detector common voltage Detector bias = VDETCOM - 4.7*

\* VDETCOM lower than 4.7 V will forward bias the sensor, the exact zero bias voltage is device and temperature dependent.

### Digital Pattern Input

Pin #	Clocks	Levels	Rise/Fall	Remark
5	CLK	0 V - 5.5 V	< 10 ns	Master clock Max. Freq. = 5 MHz
3	FSYNC	0 V - 5.5 V	< 10 ns	Frame sync - controls frame start and integration time
4	LSYNC	0 V - 5.5 V	< 10 ns	Line sync - controls line readout timing
2	DATA	0 V - 5.5 V	< 10 ns	Data code input - programs device function registers in Control Mode Left open in Default Mode

Clocks	Synchronization
FSYNC	Rising and falling when CLK is rising
LSYNC	Rising and falling when CLK is falling
DATA	Rising and falling when CLK is rising



## Analog video Output

Pin #	Outputs	Levels	Settle	Remark
18	OUTA	1.3 V to 4.2 V	< 50 ns to 0.1 %	Output A used in single output mode
19	OUTB	1.3 V to 4.2 V	< 50 ns to 0.1 %	Output A and B used in two output mode
20	OUTC	1.3 V to 4.2 V	< 50 ns to 0.1 %	Output A, B, C, and D used in four output mode
21	OUTD	1.3 V to 4.2 V	< 50 ns to 0.1 %	Output A, B, C, and D used in four output mode
22	OUTR	3 V	-	Reference for common mode output

## Gain & Bandwidth Selection in Default Mode

Pin #	Functions	Low	High	Remark
1	GAIN	0 V C = 10 fF	5.5 V C = 210 fF	Selects unit cell integration capacitor Left open in Control Mode
44	BWL	0V Low BW	5.5 V High BW	Selects bandwidth limiting capacitor in unit cell Left open in Control Mode

## Advanced Function

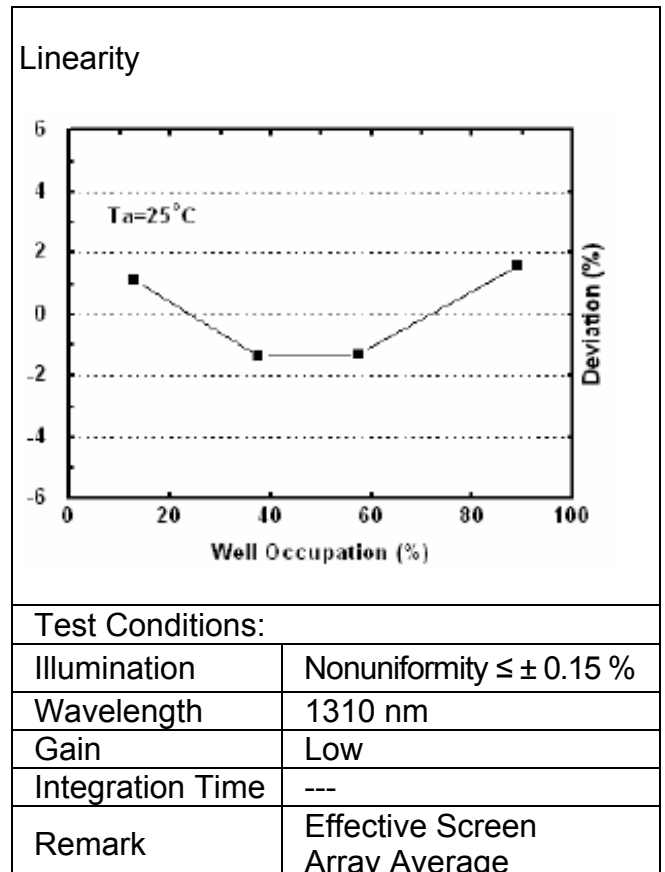
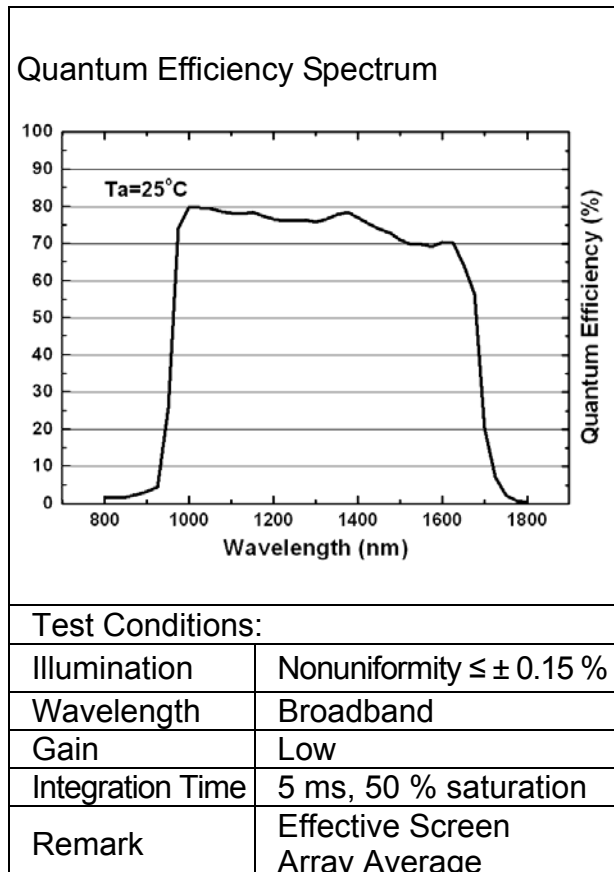
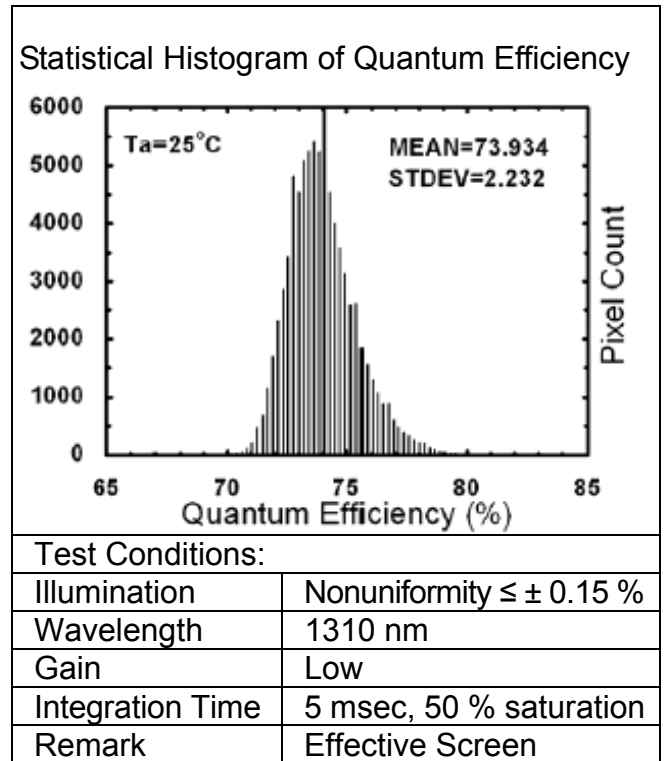
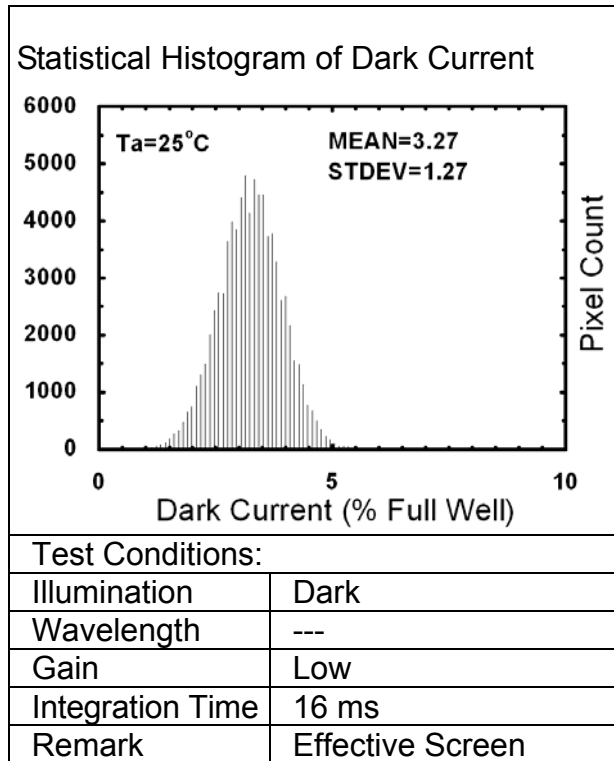
Pin #	Functions	Voltages	Remark
27	VCAS*	3.75 V	CTIA amplifier cascode FET bias
26	VOUTREF*	3 V	Output reference level during blanking period
25	VBLM*	2 V	Detector bloom control
28	IMSTR_ADJ**	0 V - 5.5 V	Adjusts analog master bias current
24	VOS	0 V - 5.5 V	Variable Offset/Skimming Control Voltage
41	TEMP	0 V - 5.5 V	On chip temperature monitor 0.74 V at 300 K, <b>Slope = -14.8 mV/10K in 50 - 300 K</b>
43	VTESTIN	1.5 V - 4.5 V	For use in IC function test
42	TESTOUT	0 V - 5.5 V	Left open in FPA operation

\* Internally generated after bias input, but can be overridden.

\*\* Also addressable through control register (DATA).

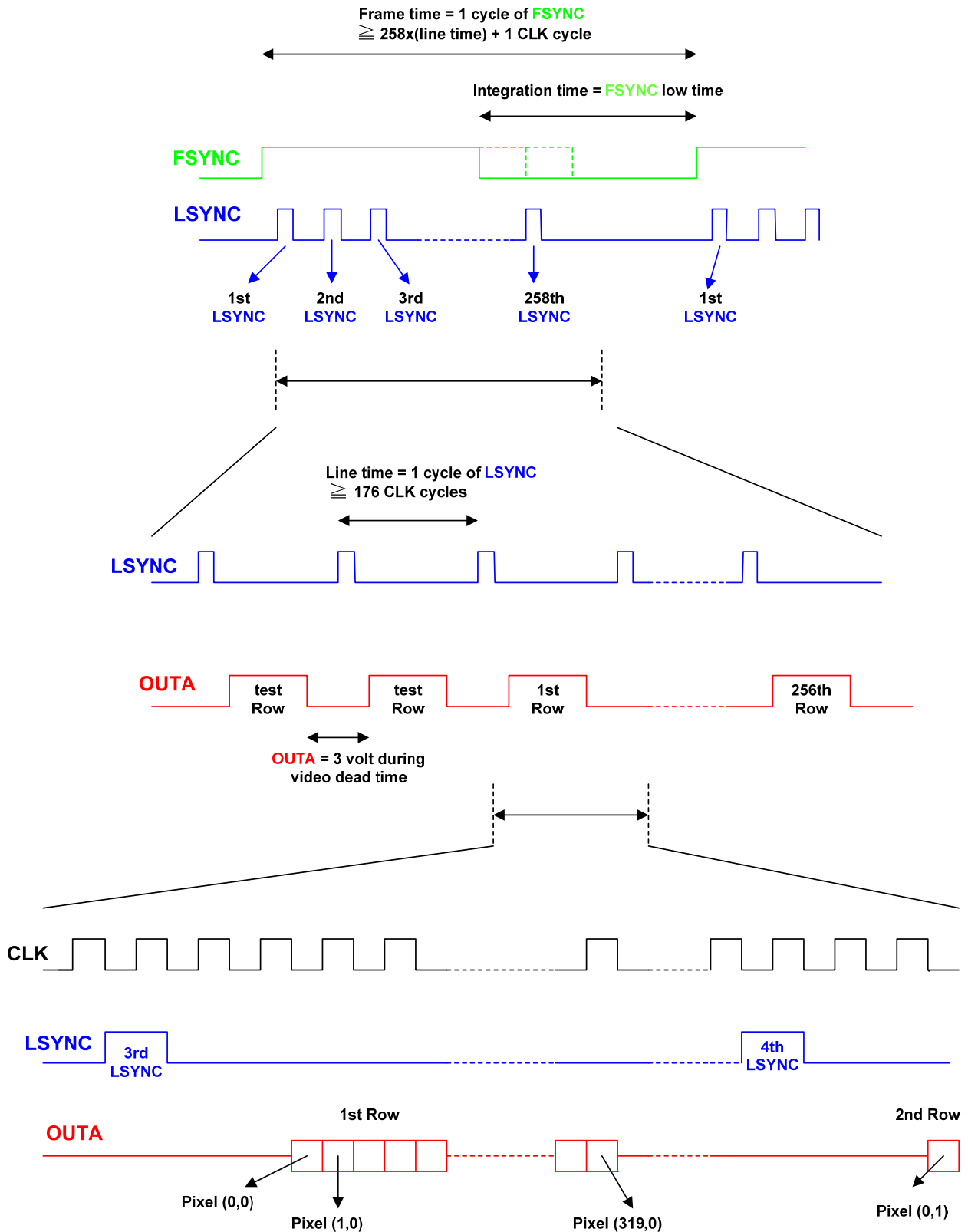


## EXAMPLE CURVES



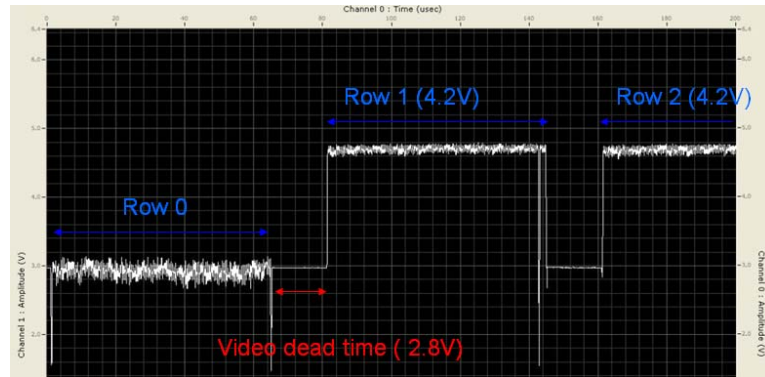


## TIMING CHART FOR DEFAULT MODE OPERATION

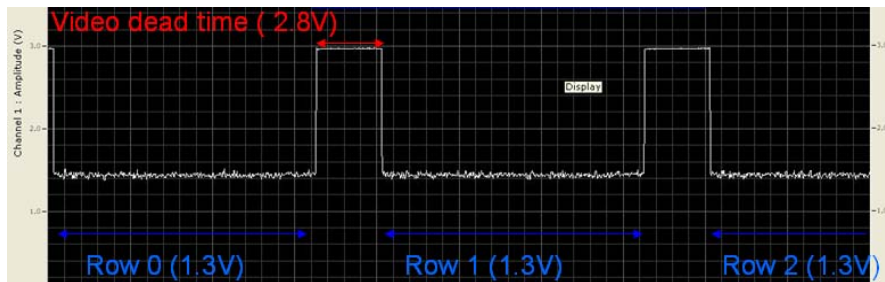




## OUTA waveform under dark



## OUTA waveform under saturation



## OUTA waveform under half saturation

