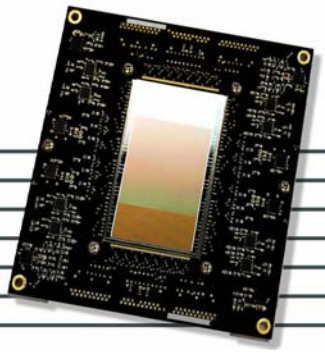


CCD_FT2K Frame Transfer CCD Image Sensor 1920 x 1920 Element Image Area

Features

- 1920 x 1920 Photosite Frame Transfer CCD Array
- 16 µm x 16 µm Pixel
- 30.72mm x 30.72mm Image Area
- 100% Fill Factor
- Readout Noise Less Than 5 Electrons at 1MHz
- Dynamic Range > 75dB
- 16 Single Stage Source Follower Output Channels
- Three-Phase Buried Channel NMOS Image area
- Three-Phase Buried Channel Readout Registers
- Multi-Pinned Phase (MPP) optional

General Description

The CCD_FT2K is a 1920 x 1920 image element solid state Charge Coupled Device (CCD) Frame Transfer sensor. This CCD is intended for use in high-resolution scientific, space based, Industrial, and commercial electro-optical systems.

The CCD_FT2K is organized in a single array of 1920 horizontal by 1920 vertical photosite image region with a 1920 x 960 vertical photosite storage region on each end of the device.

The pixel spacing is 16µm x 16µm. For dark reference, each readout line is proceeded by 4 dark pixels.

The CCD_FT2K is offered in an MPP mode frontside illuminated version for decreased dark signal.

Functional Description

The following functional elements are illustrated in the block diagram:

Image Sensing Elements: Incident photons pass through a transparent polycrystalline silicon gate structure creating electron hole pairs. The resulting photoelectrons are collected in the photosites during the integration period. The amount of charge accumulated in each photosite is a linear function of the localized incident illumination intensity and integration period.

The photosite structure is made up of contiguous CCD elements with no voids or inactive areas. In addition to sensing light, these elements are used to shift image data vertically.

Vertical Charge Shifting: The Frame Transfer architecture of the CCD_FT2K provides video information as a single sequential readout of 1920 lines containing 1920 photosites. At the end of an integration period the ΦV_1, ΦV_2, and ΦV_3 clocks are used to transfer charge vertically through the CCD array to the storage region. The vertical storage pixels then transfer charge to the horizontal readout register. Vertical columns are separated by a channel stop region to prevent charge migration.

Horizontal Charge Shifting ΦS_1, ΦS_2 and ΦS_3 are polysilicon gates used to transfer charge horizontally to the output amplifier. The horizontal transport register is twice the size of the photosite to allow for vertical binning. For frame transfer configurations, the charge must be read out through the eight amplifiers at the bottom and the eight amplifiers at the top of the image frame storage region.

The transfer of charge into the horizontal register is the result of a vertical shift sequence. This register has 4 additional register cells between the first pixel of each line and the output amplifier. The output from these locations contains no signal and may be used as a dark level reference.

The last clocked gate in the Horizontal registers is twice as large as the others and can be used to horizontally bin charge. This gate requires its own clock, which may be tied to ΦS_1 for normal full resolution readout.

The reset FET in the horizontal readout, clocked appropriately with ΦR, allows binning of adjacent pixels.

Output Amplifier: The CCD_FT2K has 16 output amplifiers evenly distributed along each Horizontal register. They are single stage FET floating diffusion amplifiers with a reset MOSFET tied to the input gate.

Charge packets are clocked to a pre-charged capacitor whose potential changes linearly in response to the number of electrons delivered. When this potential is applied to the input gate of an NMOS amplifier, a signal, V_{out}, at the output pin is produced. The capacitor is then reset via the reset MOSFET with ΦR to a precharge level prior to the arrival of the next charge packet except when horizontally binning. The output amplifier drain is tied to VDD.

The source is connected to an external load resistor to ground and constitutes the video output from the device.

Definition of Terms

Charge-Coupled Device A charge-coupled device is a monolithic silicon structure in which discrete packets of electron charge are transported from position to position by sequential clocking of an array of gates.

Vertical Transport Clocks ΦV_1, ΦV_2, ΦV_3 the clock signals applied to the vertical transport register. The nomenclature used is AI1, AI2, and AI3 for the image sections and AS1, AS2, and AS3 for the storage sections of the CCD.

Horizontal Transport Clocks ΦS_1, ΦS_2, ΦS_3 the clock signals applied to the horizontal transport registers. The nomenclature used is S1, S2, and S3.

Reset Clock ΦR the clock applied to the reset switch of the output amplifier.

Dynamic Range The ratio of saturation output voltage to RMS noise in the dark. The peak-to-peak random noise is 4-6 times the RMS noise output.

Saturation Exposure The minimum exposure level that produces an output signal corresponding to the maximum photosite charge capacity. Exposure is equal to the product of light intensity and integration time.

Responsivity The output signal voltage per unit of exposure.

Spectral Response Range The spectral band over which the response per unit of radiant power is more than 10% of the peak response.

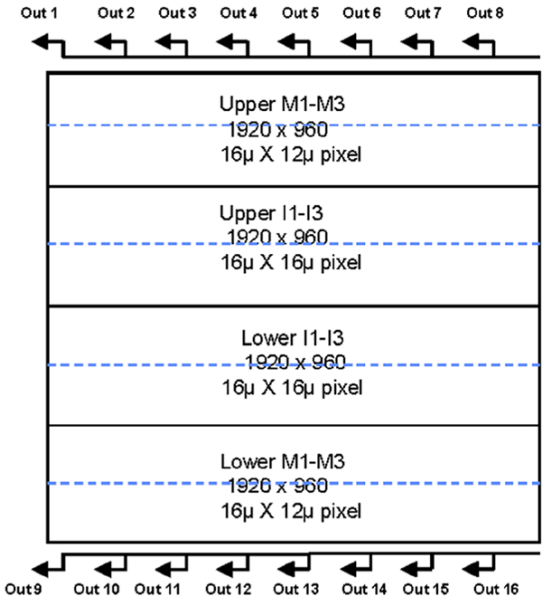
Photo-Response Non-Uniformity The difference of the response levels between the most and the least sensitive regions under uniform illumination (excluding blemished elements) expressed as a percentage of the average response.

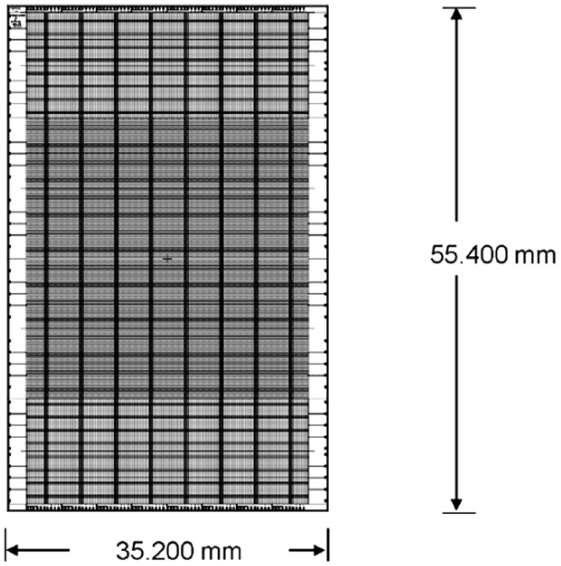
Dark Signal The output signal is caused by thermally generated electrons. Dark signal is a linear function of integration time and an exponential function of chip temperature.

Vertical Transfer Gate ΦVTG Gate structures adjacent to the end row of photosites and the horizontal transport registers. The charge packets accumulated in the photosites are shifted vertically through the array. Upon reaching the end row of photosites, the charge is transferred in parallel via the transfer gates to the horizontal transport shift registers whenever the transfer gate voltage goes low.

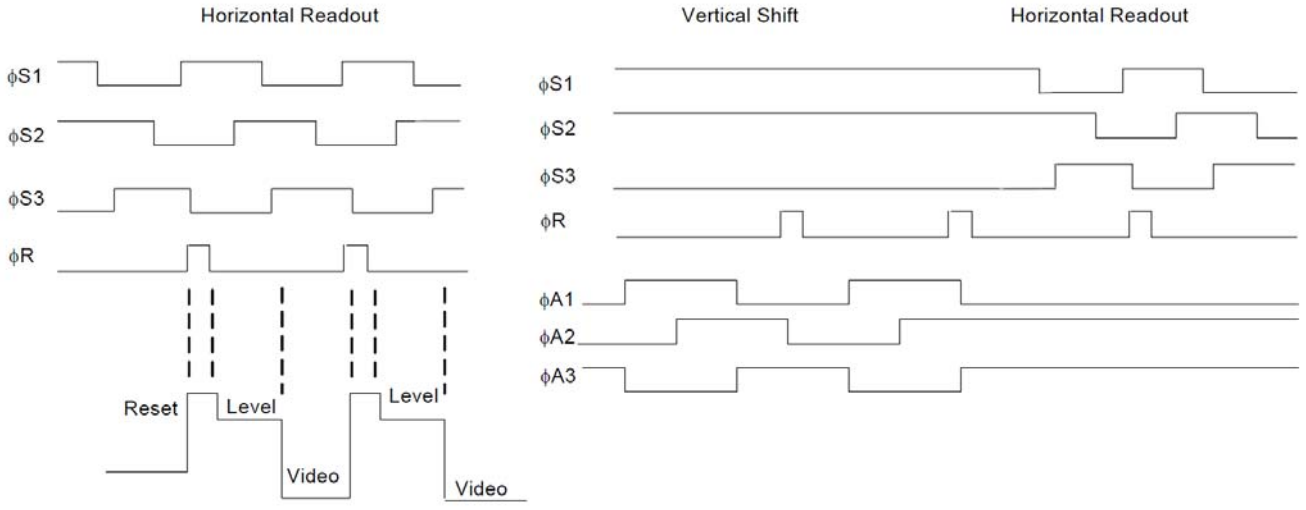
Pixel Picture element or sensor element, also called photo element or photosite.

CCD Block Diagram





Timing Diagram



TYPICAL CCD DC OPERATING CHARACTERISTICS

Symbol	Parameter	Range min	Range nom	Range max	Unit	Remarks
V_{DD}	DC Supply Voltage		25.0		V	
V_{RD}	Reset Drain Voltage		16.0		V	
V_{OTG}	Output Transfer Voltage	-2.0	1.0	2.0	V	
V_{GND}	Substrate Ground		0.0		V	
V_{SC}	Scupper		20.0		V	

Typical Clock Voltages

Symbol	Parameter	High	Low	Unit	Remarks
$V\phi_{S(1,2,3)}$	Horizontal Multiplexer Clock	+5.0	-5.0	V	Note 1
$V\phi_{SG}$	Summing Gate Clock	+5.0	-5.0	V	Note 1
$V\phi_{V(1,2,3)}$	Vertical Array Clocks	+3.0	-10.0	V	Note 1
$V\phi_{RG}$	Reset Gate Clock	+8.0	-2.0	V	Note 1

Note 1: ϕS = 200pF, ϕV = 15,000pF. All clock rise and fall times should be < 10 ns.

AC Characteristics

Symbol	Parameter	Range min	Range nom	Range max	Unit	Remarks
V_{ODC}	Output DC Level		17.0		V	
Z	Suggested Load Resistor	1.0	5.0	20.0	kΩ	

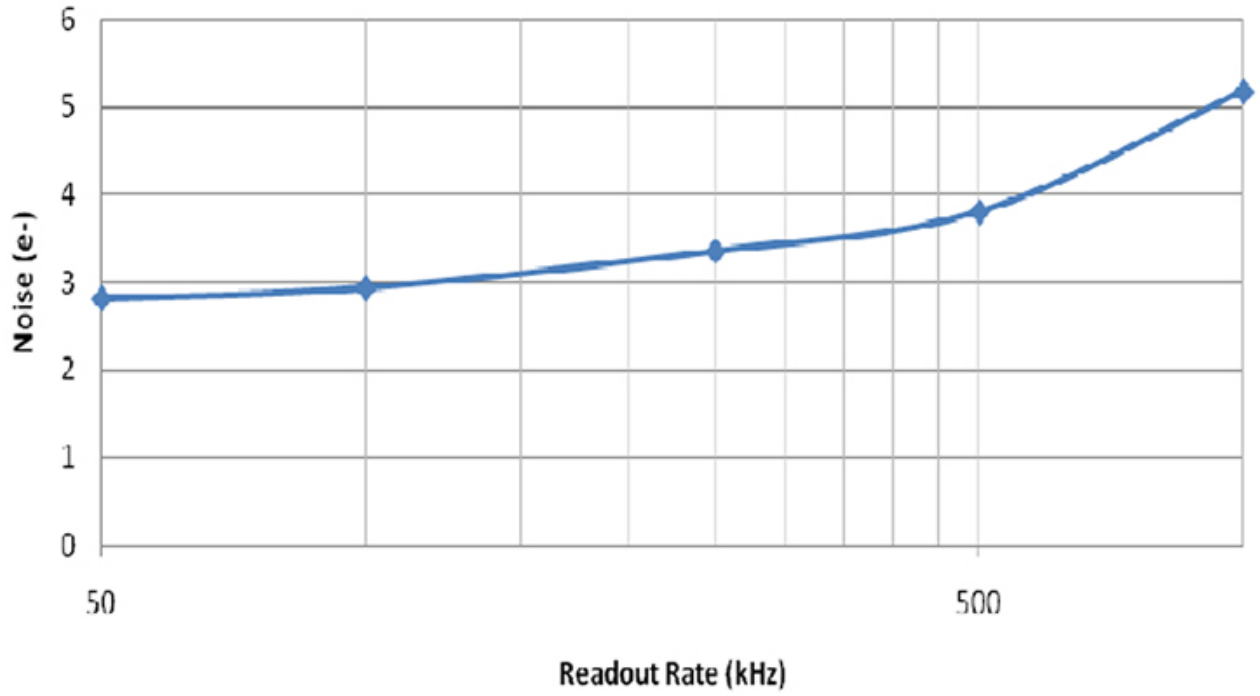
Standard test conditions are nominal MPP clocks and DC operating Voltages, 1 MHz Horizontal Data Rate, 6µSec Vertical shift cycle.

Performance Specifications

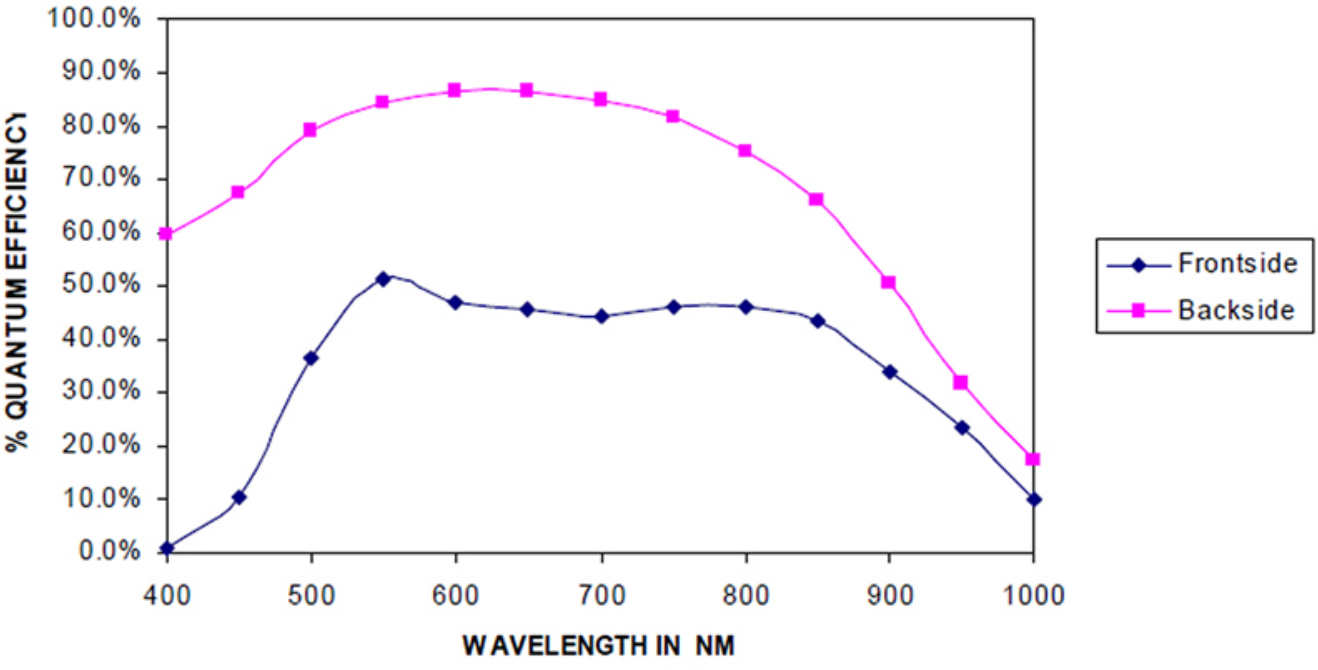
Symbol	Parameter	Range min	Range nom	Range max	Unit	Remarks
V_{SAT}	Saturation Output Voltage Full Well Capacity Output Amp Sensitivity	125K	700 180K 4.0	220K	mV e- µV/e-	Note 1
PRNU	Photo Response Non-Uniformity Peak-to-Peak		10		$\%V_{SAT}$	
DSNU	Dark Signal Non-Uniformity Peak-to-Peak			1.0	mV	
DC	Dark Current	0.025	<1.0	2.0	nA/cm^2	Note 2
R	Responsitivity		1.0		$V\mu j/cm^2$	
Rms	Noise		3 -20		e-	

Note 1: Maximum well capacity is achieved in Buried Channel Mode.
Note 2: Values shown are for 25°C. Dark current doubles for every 5°- 7°C.

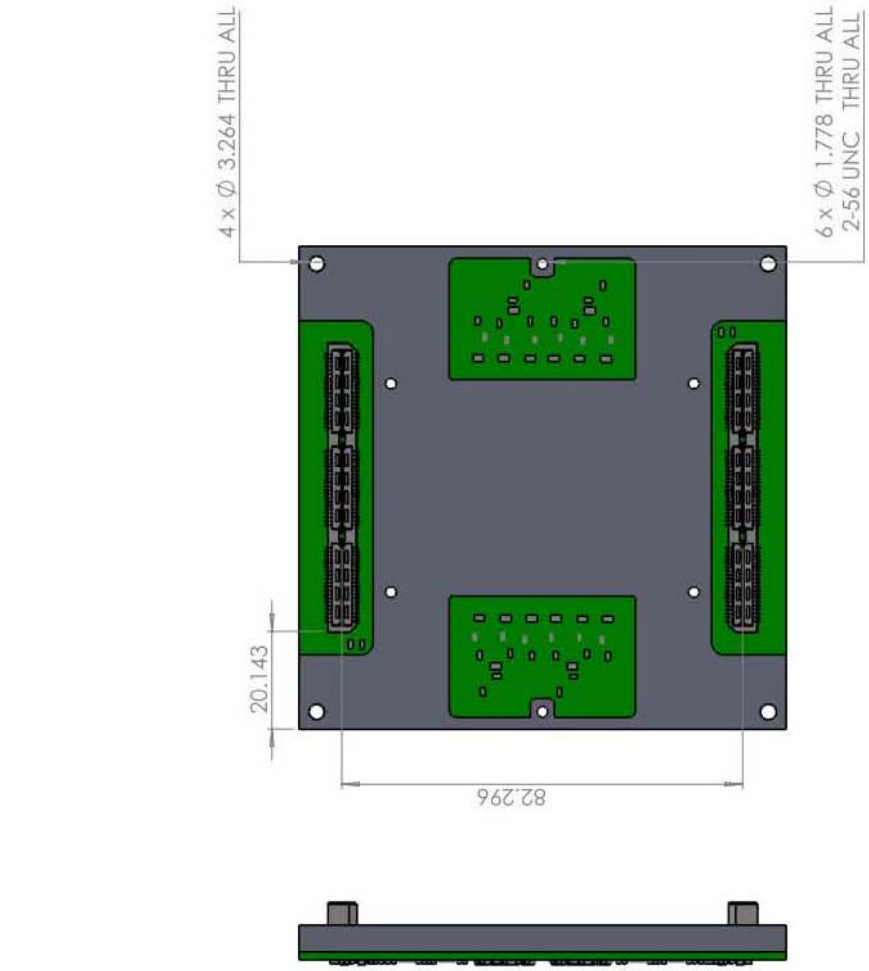
Typical RMS Noise (e-)

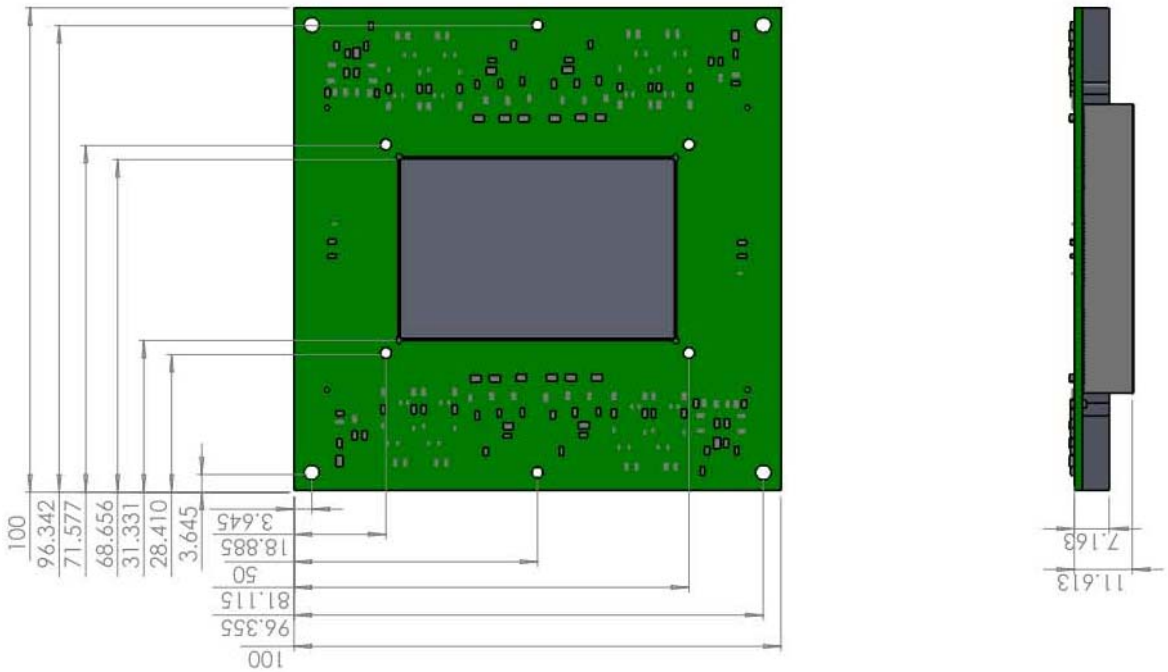


Typical CCD Quantum Efficiency

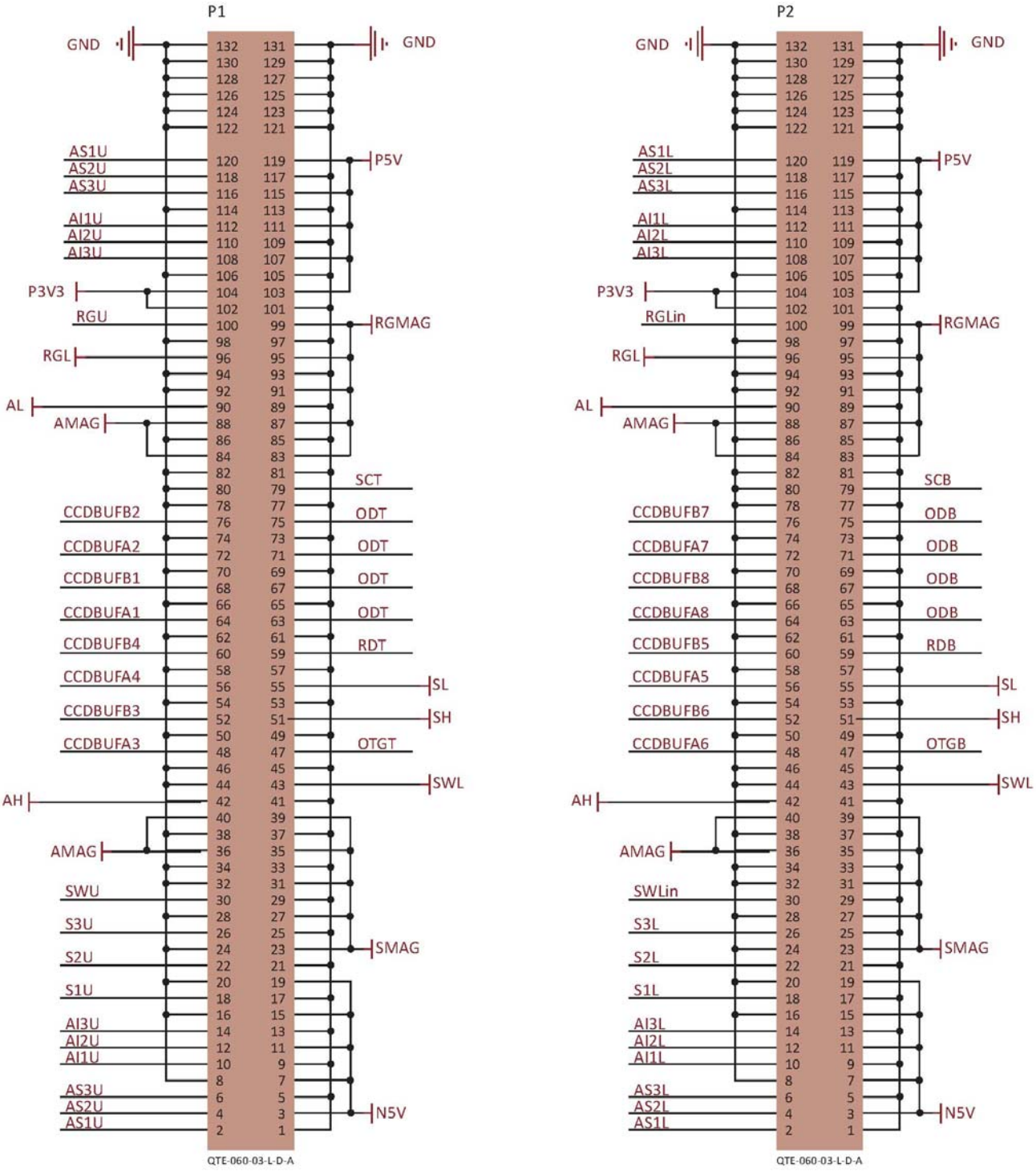


CCD_FT2K Package





CCD_FT2K Package Pin Configuration



	Connector	Connector Pin	Pin Label	Function	Value
	P1	1	GND	Ground	0V
		2	AS1U	Upper Storage 1 TTL Clock	0V to 5V
		3	N5V	Negative Voltage Logic	-5V
		4	AS2U	Upper Storage 2 TTL Clock	0V to 5V
		5	GND	Ground	0V
		6	AS3U	Upper Storage 3 TTL Clock	0V to 5V
		7	N5V	Negative Voltage Logic	-5V
		8	GND	Ground	0V
		9	GND	Ground	0V
		10	AI1U	Upper Image Phase1 TTL Clock	0V to 5V
		11	N5V	Negative Voltage Logic	-5V
		12	AI2U	Upper Image Phase2 TTL Clock	0V to 5V
		13	GND	Ground	0V
		14	AI3U	Upper Image Phase3 TTL Clock	0V to 5V
		15	N5V	Negative Voltage Logic	-5V
		16	GND	Ground	0V
		17	GND	Ground	0V
		18	S1U	Upper Serial Phase1 TTL Clock	0V to 5V
		19	N5V	Negative Voltage Logic	-5V
		20	GND	Ground	0V
		21	GND	Ground	0V
		22	S2U	Upper Serial Phase2 TTL Clock	0V to 5V
		23	SMAG	Serial Magnitude Voltage	10V
		24	GND	Ground	0V
		25	GND	Ground	0V
		26	S3U	Upper Serial Phase3 TTL Clock	0V to 5V
		27	SMAG	Serial Magnitude Voltage	10V
		28	GND	Ground	0V
		29	GND	Ground	0V
		30	SWU	Upper Summing Well TTL Clock	0V to 5V
		31	SMAG	Serial Magnitude Voltage	10V
		32	GND	Ground	0V
		33	GND	Ground	0V
		34	GND	Ground	0V
		35	SMAG	Serial Magnitude Voltage	10V
		36	AMAG	Array Magnitude Voltage	13V
		37	GND	Ground	0V
		38	GND	Ground	0V
		39	SMAG	Serial Magnitude Voltage	10V
		40	AMAG	Array Magnitude Voltage	13V
		41	GND	Ground	0V
		42	AH	Array Clock Static High Level	3V
		43	SWL	Summing Well Clock Static Low Level	-5V
		44	GND	Ground	0V
		45	GND	Ground	0V
		46	GND	Ground	0V
		47	OTGT	Output Transfer Gate Voltage	-1V
		48	CCDBUFA3	CCD Buffered Output	--
		49	GND	Ground	0V

		50	GND	Ground	0V
		51	SH	Serial Clock Static High Level	5V
		52	CCDBUFB3	CCD Buffered Output	--
		53	GND	Ground	0V
		54	GND	Ground	0V
		55	SL	Serial Clock Static Low Level	-5V
		56	CCDBUFA4	CCD Buffered Output	--
		57	GND	Ground	0V
		58	GND	Ground	0V
		59	RDT	Reset Drain Voltage	16V
		60	CCDBUFB4	CCD Buffered Output	--
		61	GND	Ground	0V
		62	GND	Ground	0V
		63	ODT	Output Drain Voltage	25V
		64	CCDBUFA1	CCD Buffered Output	--
		65	GND	Ground	0V
		66	GND	Ground	0V
		67	ODT	Output Drain Voltage	25V
		68	CCDBUFB1	CCD Buffered Output	--
		69	GND	Ground	0V
		70	GND	Ground	0V
		71	ODT	Output Drain Voltage	25V
		72	CCDBUFA2	CCD Buffered Output	--
		73	GND	Ground	0V
		74	GND	Ground	0V
		75	ODT	Output Drain Voltage	25V
		76	CCDBUFB2	CCD Buffered Output	--
		77	GND	Ground	0V
		78	GND	Ground	0V
		79	SCT	Scupper Voltage	20V
		80	GND	Ground	0V
		81	GND	Ground	0V
		82	GND	Ground	0V
		83	RGMAG	Reset Clock Magnitude Voltage	10V
		84	AMAG	Array Magnitude Voltage	13V
		85	GND	Ground	0V
		86	GND	Ground	0V
		87	RGMAG	Reset Clock Magnitude Voltage	10V
		88	AMAG	Array Magnitude Voltage	13V
		89	GND	Ground	0V
		90	AL	Array Clock Static Low Level	-10V
		91	RGMAG	Reset Clock Magnitude Voltage	10V
		92	GND	Ground	0V
		93	GND	Ground	0V
		94	GND	Ground	0V
		95	RGMAG	Reset Clock Magnitude Voltage	10V
		96	RGL	Reset Clock Static Low Level	-2V
		97	GND	Ground	0V
		98	GND	Ground	0V
		99	RGMAG	Reset Clock Magnitude Voltage	10V
		100	RGU	Reset Gate TTL Clock	0V to 5V

		101	GND	Ground	0V
		102	P3V3	Positive Voltage Reset Driver	3.3V
		103	P5V	Positive Voltage Logic	5V
		104	P3V3	Positive Voltage Reset Driver	3.3V
		105	GND	Ground	0V
		106	GND	Ground	0V
		107	P5V	Positive Voltage Logic	5V
		108	AI3U	Upper Image Phase3 TTL Clock	0V to 5V
		109	GND	Ground	0V
		110	AI2U	Upper Image Phase2 TTL Clock	0V to 5V
		111	P5V	Positive Voltage Logic	5V
		112	Al1U	Upper Image Phase1 TTL Clock	0V to 5V
		113	GND	Ground	0V
		114	GND	Ground	0V
		115	PSV	Positive Voltage Logic	5V
		116	AS3U	Upper Storage Phase3 TTL Clock	0V to 5V
		117	GND	Ground	0V
		118	AS2U	Upper Storage Phase2 TTL Clock	0V to 5V
		119	P5V	Positive Voltage Logic	5V
		120	AS1U	Upper Storage Phase1 TTL Clock	0V to 5V
		121	GND	Ground	0V
		122	GND	Ground	0V
		123	GND	Ground	0V
		124	GND	Ground	0V
		125	GND	Ground	0V
		126	GND	Ground	0V
		127	GND	Ground	0V
		128	GND	Ground	0V
		129	GND	Ground	0V
		130	GND	Ground	0V
		131	GND	Ground	0V
		132	GND	Ground	0V

	Connector	Connector Pin	Pin Label	Function	Value
	P2	1	GND	Ground	0V
		2	AS1L	Lower Storage 1 TTL Clock	0V to 5V
		3	N5V	Negative Voltage Logic	-5V
		4	AS2L	Lower Storage 2 TTL Clock	0V to 5V
		5	GND	Ground	0V
		6	AS3L	Lower Storage 3 TTL Clock	0V to 5V
		7	N5V	Negative Voltage Logic	-5V
		8	GND	Ground	0V
		9	GND	Ground	0V
		10	Al1L	Lower Image Phase1 TTL Clock	0V to 5V
		11	N5V	Negative Voltage Logic	-5V
		12	AI2L	Lower Image Phase2 TTL Clock	0V to 5V
		13	GND	Ground	0V
		14	AI3L	Lower Image Phase3 TTL Clock	0V to 5V
		15	N5V	Negative Voltage Logic	-5V
		16	GND	Ground	0V

		17	GND	Ground	0V
		18	S1L	Upper Serial Phase1 TTL Clock	0V to 5V
		19	N5V	Negative Voltage Logic	-5V
		20	GND	Ground	0V
		21	GND	Ground	0V
		22	S2L	Lower Serial Phase2 TTL Clock	0V to 5V
		23	SMAG	Serial Magnitude Voltage	10V
		24	GND	Ground	0V
		25	GND	Ground	0V
		26	S3L	Lower Serial Phase3 TTL Clock	0V to 5V
		27	SMAG	Serial Magnitude Voltage	10V
		28	GND	Ground	0V
		29	GND	Ground	0V
		30	SWLin	Lower Summing Well TTL Clock	0V to 5V
		31	SMAG	Serial Magnitude Voltage	10V
		32	GND	Ground	0V
		33	GND	Ground	0V
		34	GND	Ground	0V
		35	SMAG	Serial Magnitude Voltage	10V
		36	AMAG	Array Magnitude Voltage	13V
		37	GND	Ground	0V
		38	GND	Ground	0V
		39	SMAG	Serial Magnitude Voltage	10V
		40	AMAG	Array Magnitude Voltage	13V
		41	GND	Ground	0V
		42	AH	Array Clock Static High Level	3V
		43	SWL	Summing Well Clock Static Low Level	-5V
		44	GND	Ground	0V
		45	GND	Ground	0V
		46	GND	Ground	0V
		47	OTGB	Output Transfer Gate Voltage	-1V
		48	CCDBUFA6	CCD Buffered Output	--
		49	GND	Ground	0V
		50	GND	Ground	0V
		51	SH	Serial Clock Static High Level	5V
		52	CCDBUFB6	CCD Buffered Output	--
		53	GND	Ground	0V
		54	GND	Ground	0V
		55	SL	Serial Clock Static Low Level	-5V
		56	CCDBUFA5	CCD Buffered Output	--
		57	GND	Ground	0V
		58	GND	Ground	0V
		59	RDB	Reset Drain Voltage	16V
		60	CCDBUFB5	CCD Buffered Output	--
		61	GND	Ground	0V
		62	GND	Ground	0V
		63	ODB	Output Drain Voltage	25V
		64	CCDBUFA8	CCD Buffered Output	--
		65	GND	Ground	0V
		66	GND	Ground	0V
		67	ODB	Output Drain Voltage	25V

		68	CCDBUFB8	CCD Buffered Output	--
		69	GND	Ground	0V
		70	GND	Ground	0V
		71	ODB	Output Drain Voltage	25V
		72	CCDBUFA7	CCD Buffered Output	--
		73	GND	Ground	0V
		74	GND	Ground	0V
		75	ODB	Output Drain Voltage	25V
		76	CCDBUFB7	CCD Buffered Output	--
		77	GND	Ground	0V
		78	GND	Ground	0V
		79	SCB	Scupper Voltage	20V
		80	GND	Ground	0V
		81	GND	Ground	0V
		82	GND	Ground	0V
		83	RGMAG	Reset Clock Magnitude Voltage	10V
		84	AMAG	Array Magnitude Voltage	13V
		85	GND	Ground	0V
		86	GND	Ground	0V
		87	RGMAG	Reset Clock Magnitude Voltage	10V
		88	AMAG	Array Magnitude Voltage	13V
		89	GND	Ground	0V
		90	AL	Array Clock Static Low Level	-10V
		91	RGMAG	Reset Clock Magnitude Voltage	10V
		92	GND	Ground	0V
		93	GND	Ground	0V
		94	GND	Ground	0V
		95	RGMAG	Reset Clock Magnitude Voltage	10V
		96	RGL	Reset Clock Static Low Level	-2V
		97	GND	Ground	0V
		98	GND	Ground	0V
		99	RGMAG	Reset Clock Magnitude Voltage	10V
		100	RGLin	Reset Gate TTL Clock	0V to 5V
		101	GND	Ground	0V
		102	P3V3	Positive Voltage Reset Driver	3.3V
		103	P5V	Positive Voltage Logic	5V
		104	P3V3	Positive Voltage Reset Driver	3.3V
		105	GND	Ground	0V
		106	GND	Ground	0V
		107	P5V	Positive Voltage Logic	5V
		108	AI3L	Lower Image Phase3 TTL Clock	0V to 5V
		109	GND	Ground	OV
		110	AI2L	Lower Image Phase2 TTL Clock	0V to 5V
		111	P5V	Positive Voltage Logic	5V
		112	AI1L	Lower Image Phase1 TTL Clock	0V to 5V
		113	GND	Ground	0V
		114	GND	Ground	0V
		115	P5V	Positive Voltage Logic	5V
		116	AS3L	Lower Storage Phase3 TTL Clock	0V to 5V
		117	GND	Ground	0V
		118	AS2L	Lower Storage Phase2 TTL Clock	0V to 5V

		119	P5V	Positive Voltage Logic	5V
		120	AS1L	Lower Storage Phase1 TTL Clock	0V to 5V
		121	GND	Ground	0V
		122	GND	Ground	0V
		123	GND	Ground	0V
		124	GND	Ground	0V
		125	GND	Ground	0V
		126	GND	Ground	0V
		127	GND	Ground	0V
		128	GND	Ground	0V
		129	GND	Ground	0V
		130	GND	Ground	0V
		131	GND	Ground	0V
		132	GND	Ground	0V

Quantum Efficiency Enhancements

The CCD_FT2K CCD area arrays can be backside thinned for increased QE. The incident illumination enters through the backside of the array, and since no photons are absorbed in the polysilicon gate structures, the QE is increased. Also available are front side illuminated devices which can be coated with a fluorescent dye that absorbs UV light and fluoresces in the visible range. This provides CCD response at wavelengths less than 400nm.

Cosmetic Grading

Device grading helps to establish a ranking for the image quality that a CCD will provide. Blemishes are characterized as spurious pixels exceeding 10% of V_{SAT} with respect to neighboring elements. Blemish content is determined in the dark, at various illumination levels, and for different device temperatures.

The CCD_FT2K is available in various standard grades, as well as custom selected grades. Consult ANDANTA GmbH for available grading information and custom selections.

Warranty

Within twelve months of delivery to the end customer ANDANTA GmbH will repair or replace, at our option, any image sensor product if any part is found to be defective in materials or workmanship. Contact ANDANTA GmbH for assignment of warranty return number and shipping instructions to ensure prompt repair or replacement.

Certification

ANDANTA GmbH certifies that all products are carefully inspected and tested prior to shipment and will meet all of the specification requirements under which it is furnished.

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