

CCD2700A CCD Image Sensor 8064 x 8064 Element Image Area

Features

- 8064 x 8064 CCD Image Array
- 7.5 μm x 7.5 μm Pixel
- 61.66 mm x 65mm Device Area
- Near 100% Fill Factor
- Readout Noise Less Than 5 Electrons at 150KHz
- 8 Dual Stage 20MHz Outputs
- Three-Phase Buried Channel NMOS Image Area
- Multi-pinned Phase (MPP)
- Three-Phase Buried Channel Readout Registers

General Description

The CCD2700A is an 8064 x 8064 pixel solid state Charge Coupled Device (CCD) imaging sensor. This CCD is intended for use in high-resolution scientific, space based, industrial, and commercial electro-optical systems. The CCD2700A is organized in two halves each containing an array of 8064 horizontal by 4032 vertical pixels. The CCD2700A may be operated in either buried-channel or MPP mode. Each pixel is 7.5 μm x 7.5 μm . For dark reference, each readout line is preceded by 8 prescan pixels. The dual stage output architecture coupled with eight readout sections allows higher frame rate operation. The CCD2700A is also offered as a backside illuminated version for increased sensitivity and UV response in the same package configuration.

Functional Description

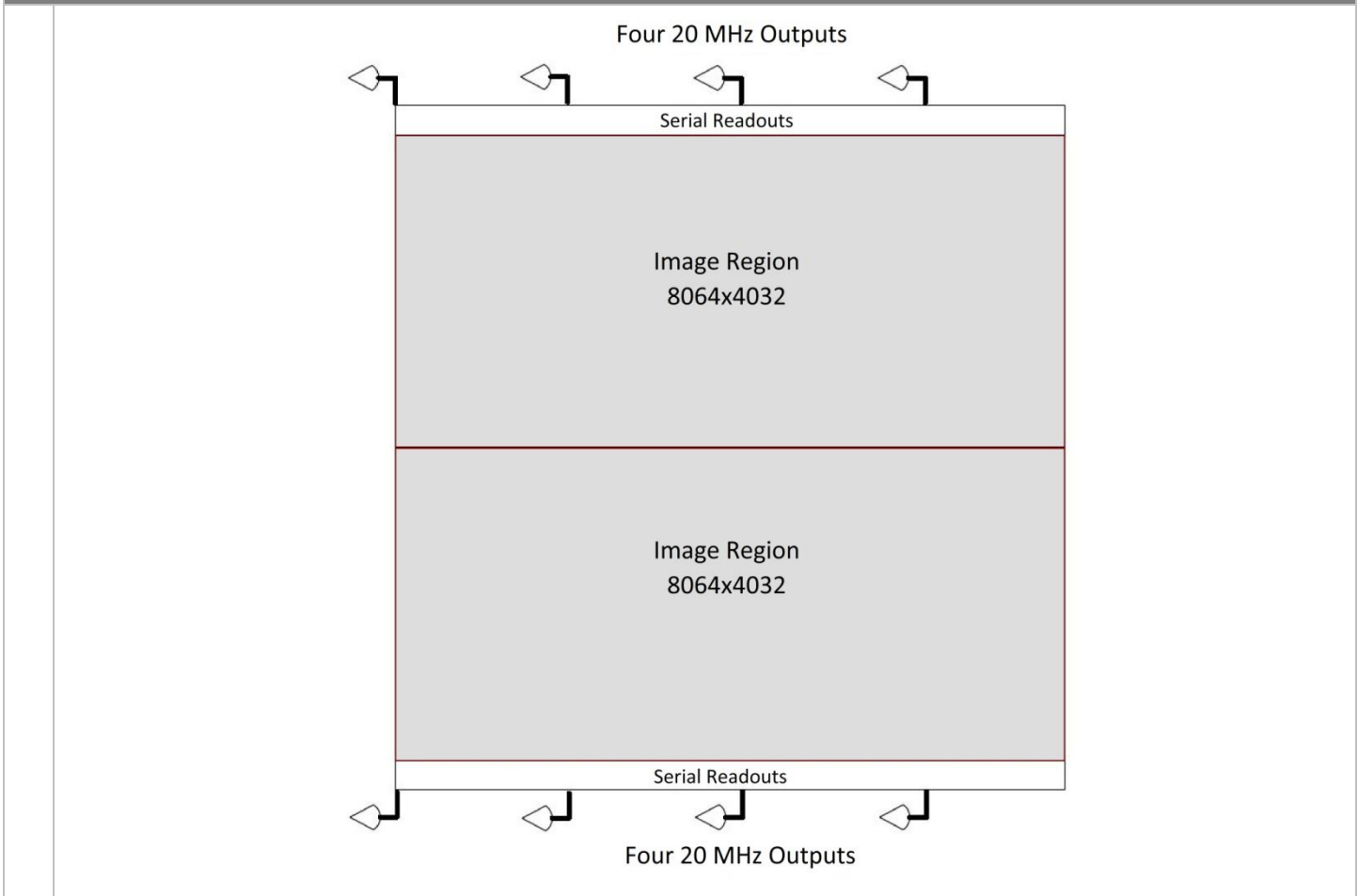
Image Sensing Elements: Incident photons pass through a transparent polycrystalline silicon gate structure and generate electrons in a pixel. There is a linear relationship between the number of electrons accumulated in each pixel, the incident illumination intensity and the integration time.

The pixel structure is a series of closely spaced MOS capacitors. The pixels convert light to electrons and then move the collected electrons vertically by shifting the potential wells created by the vertical array clocks.

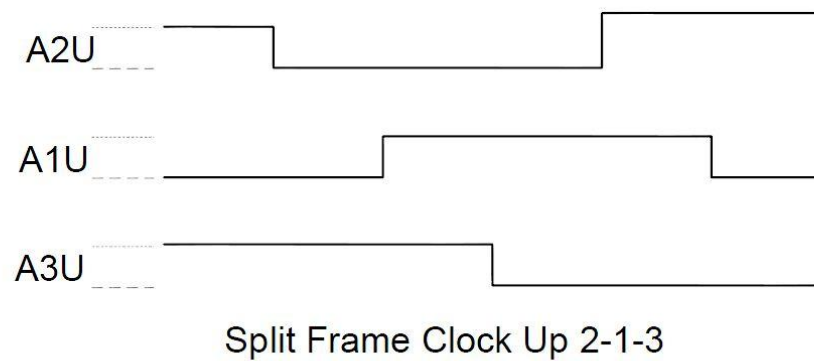
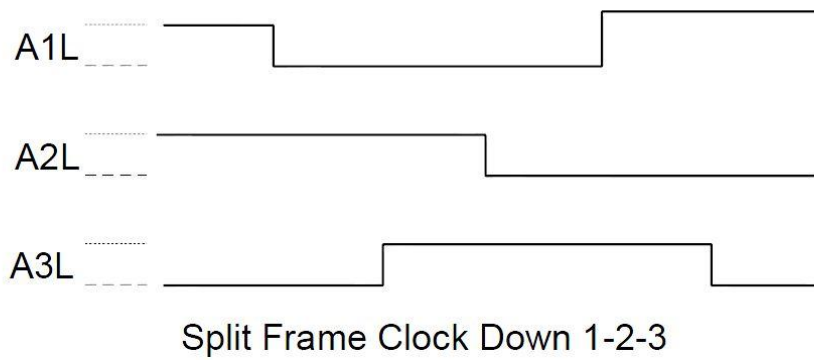
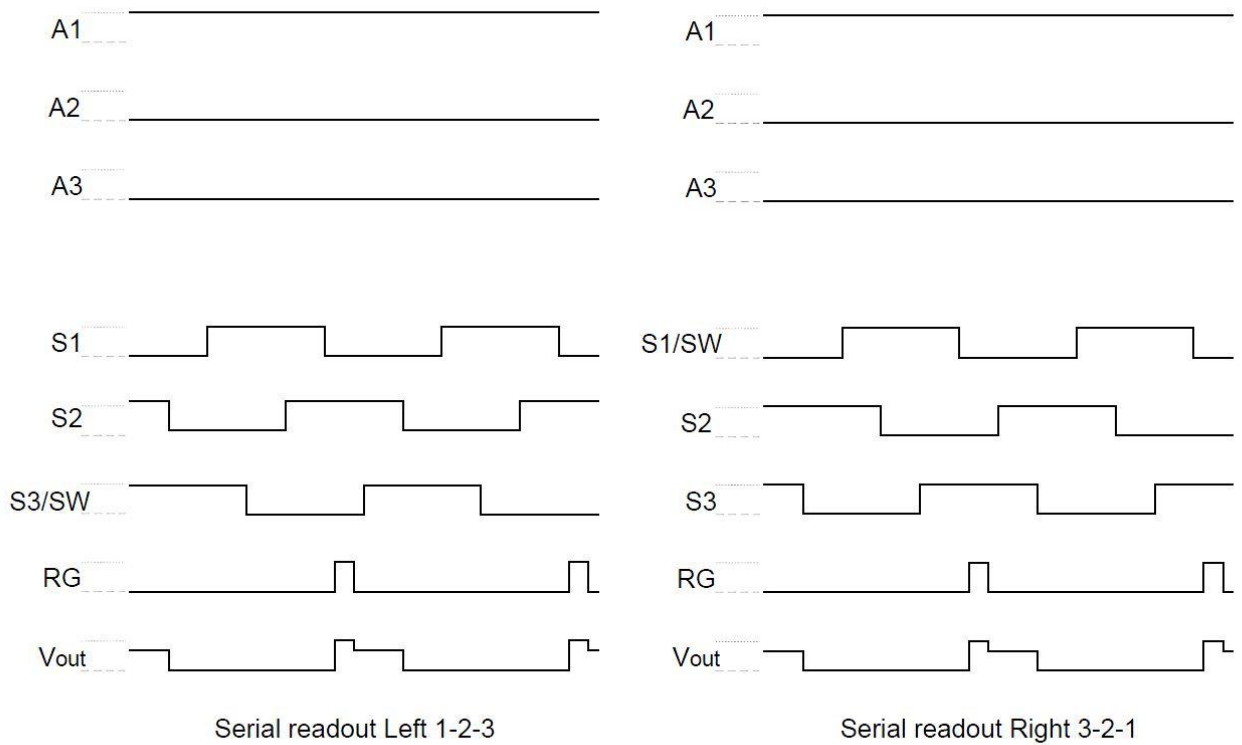
Vertical (Area) Charge Transfer: Each pixel has 3 gates, clocked by A1, A2, and A3. The charge stored under the gates may be shifted in one of three ways, split frame transfer to outputs 1-8, single frame transfer to outputs 1-4 at the top, or single frame transfer to outputs 5-8 at the bottom. At the end of an integration period the A1, A2, and A3 clocks are used to transfer charge vertically through the CCD array to the horizontal readout registers. Vertical columns are separated by a channel stop region to prevent horizontal charge migration.

	<p>The imaging area is divided into upper and lower halves. Each 8064 x 4032 section may be clocked independently or together. Horizontal registers along the top and bottom permit simultaneous readout of both halves. The CCD2700A may also be clocked such that the full array is read out by the upper or lower horizontal register alone.</p>
	<p>Horizontal (Serial) Charge Transfer: S1, S2 and S3 are polysilicon gates used to transfer charge horizontally to the output amplifiers. The horizontal register pixels are twice the size of a pixel in the image area to allow for vertical binning.</p> <p>The transfer of charge into the horizontal register is the result of a vertical shift sequence. The horizontal register has 8 additional pixels between the first pixel of each line and the output amplifier. The output from these locations contains no signal and may be used as a dark level reference.</p> <p>The last clocked gate in the horizontal registers is twice as large as the others and can be used to bin charge horizontally (this gate is called the summing well). This gate has its own clock (SW), but it can be tied to the next ordered serial clock for non-binned readout modes.</p>
	<p>Output Amplifier: The CCD2700A has eight dual stage source follower outputs that have proven low noise performance. There are four outputs for each horizontal register.</p> <p>The output capacitor (sense node) is reset via the reset MOSFET with the RG clock to a pre-charge level (RD) prior to the arrival of the next charge packet (except when horizontally binning).</p> <p>The output amplifier drains are tied to OD. The source (OS) is connected to an external load resistor to ground and constitutes the video output from the device. The output voltage changes linearly in response to the number of electrons delivered to the sense node.</p>

CCD Layout



Clock Waveforms



DC Operating Characteristics

Symbol	Parameter	Range			Unit	Remarks
		min	nom	max		
OD	DC Supply Voltage	20.0	24.0	30.0	V	
RD	Reset Drain Voltage	10.0	15.0	20.0	V	
OTG	Output Transfer Gate Voltage	-5.0	-1.0	5.0	V	
Vss	Substrate Ground	0.0			V	

Typical Clock Voltages

Symbol	Parameter	High	Low	Unit	Remarks
S1,S2,S3	Horizontal Serial Clocks	+5.0	-5.0	V	Typical clock range
SW	Summing Gate Clock	+5.0	-5.0	V	Clock as S1 or S3 if not clocked separately
A1,A2,A3	Vertical Array Clocks	+3.0	-9.0	V	
RG	Reset Gate Array Clock	+8.0	-2.0	V	

AC Characteristics

Symbol	Parameter	Range			Unit	Remarks
		min	nom	max		
V _{ODC}	Output DC Level		14.0		V	Typical
Z _{single}	Suggested Load Resistor	3.0	10.0	20.0	kΩ	Higher resistance reduces bandwidth

Performance Specifications

Symbol	Parameter	Range			Unit	Remarks
		min	nom	max		
V _{SAT}	Saturation Output Voltage Full Well Capacity	700		65k	mV	
	Well Capacity	30k			e-	
	Output amplifier sensitivity	7.0			μV/e-	
PRNU	Photo Response Non-Uniformity Peak-to-Peak			10	%V _{SAT}	
DSNU	Dark Signal Non-Uniformity Peak-to-Peak			1.0	mV	
CTE	Charge Transfer Efficiency	>0.99995				
DC	Dark Current	1.0			e-/pix/sec	25°C
	Output Linearity	<2%				
N _{RMS}	Readout Noise	4	6	8	e-	1MHz

Cosmetic Grading

Grading and screening of devices establishes a ranking for the image quality that a CCD provides. Blemishes are characterized as spurious pixels exceeding 10% of V_{SAT} with respect to neighbouring elements. Blemish content is determined in the dark, at various illumination levels, and for different device temperatures.

The CCD2700A CCD image sensor is available in various standard grades, as well as custom grades. Consult ANDANTA GmbH for information on grade selection.

Warranty

ANDANTA GmbH will repair or replace, at our option, any image sensor product within twelve months of delivery to the end customer, for any defect in materials or workmanship. Contact ANDANTA GmbH for further warranty information, a return number, and shipping instructions.

Certification

ANDANTA GmbH certifies that all products are carefully inspected and tested prior to shipment and will meet all of the specification requirements under the performance specifications summarized.