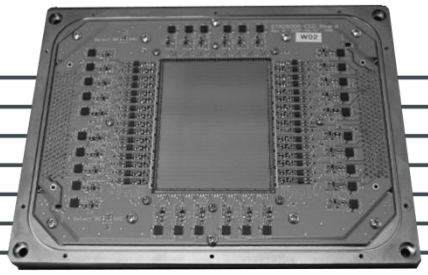


CCD2520A
4224 x 3200 Element Image Area CCD Image Sensor

Features

- 4224 x 3200 CCD Image Array
- 8.6 µm x 8.6 µm Pixel
- 36.33 mm x 27.52 Device Area
- Near 100% Fill Factor
- Readout Noise of 30 Electrons at 20MHz
- 32 Two-Stage 20MHz Outputs
- Three-Phase Buried Channel NMOS Image Area
- Three-Phase Buried Channel Readout Registers

General Description

The CCD2520A is an 4224 x 3200 pixel solid state Charge Coupled Device (CCD) imaging sensor. This CCD is intended for use in high-resolution scientific, space based, industrial, and commercial electro-optical systems. The CCD 2520A is organized in two halves each containing an array of 4244 horizontal by 1600 vertical pixels. Each pixel is 8.6 µm x 8.6 µm. For a reference dark level, each readout line is preceded by 16 prescan pixels. In addition, there are 48 columns on the left and right and 40 rows on the top and bottom masked by metal for an optical dark level. The two-stage output architecture coupled with 32 readout sections allows high frame rate operation.

Functional Description

Image Sensing Elements:

Incident photons pass through a transparent polycrystalline silicon gate structure and generate electrons in a pixel. There is a linear relationship between the number of electrons accumulated in each pixel, the incident illumination intensity and the integration time.

The pixel structure is a series of closely spaced MOS capacitors. The pixels convert light to electrons, and then move the collected electrons vertically by shifting the potential wells created by the vertical array clocks.

Vertical (Area) Charge Transfer:

Each pixel has 3 gates, clocked by A1, A2, and A3. The charge stored under the gates may be shifted in one of three ways, split frame transfer to outputs 1-32, single frame transfer to outputs 1-16 at the top, or single frame transfer to outputs 17-32 at the bottom. At the end of an integration period the A1, A2, and A3 clocks are used to transfer charge vertically through the CCD array to the horizontal readout registers. Vertical columns are separated by a channel stop region to prevent horizontal charge migration.

The imaging area is divided into upper and lower halves. Each 4224 x 1600 section may be clocked independently or together. Horizontal registers along the top and bottom permit simultaneous readout of both halves. The CCD2520A may also be clocked such that the full array is read out by the upper or lower horizontal register alone.

Horizontal (Serial) Charge Transfer:

S1, S2 and S3 are polysilicon gates used to transfer charge horizontally to the output amplifiers. The horizontal register pixels are twice the size of a pixel in the image area to allow for vertical binning.

The transfer of charge into the horizontal register is the result of a vertical shift sequence. The horizontal register has 16 additional pixels between the first active pixel of each line and the output amplifier. The output from these locations contains no signal and may be used as a dark level reference.

The last clocked gate in the horizontal registers can be used to bin charge horizontally (this gate is called the summing well). This gate has its own clock (SW), but it can be tied to the next ordered serial clock for non-binned readout modes.

Output Amplifier:

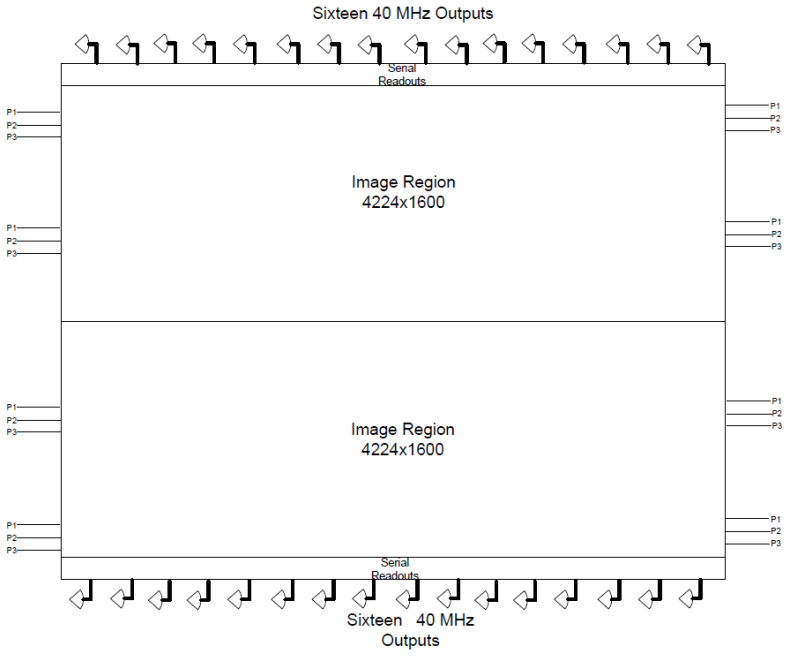
The CCD2520A has 32 two stage source follower outputs that have proven low noise performance. There are sixteen outputs for each horizontal register.

The output capacitor (sense node) is reset via the reset MOSFET with the RG clock to a pre-charge level (RD) prior to the arrival of the next charge packet (except when horizontally binning).

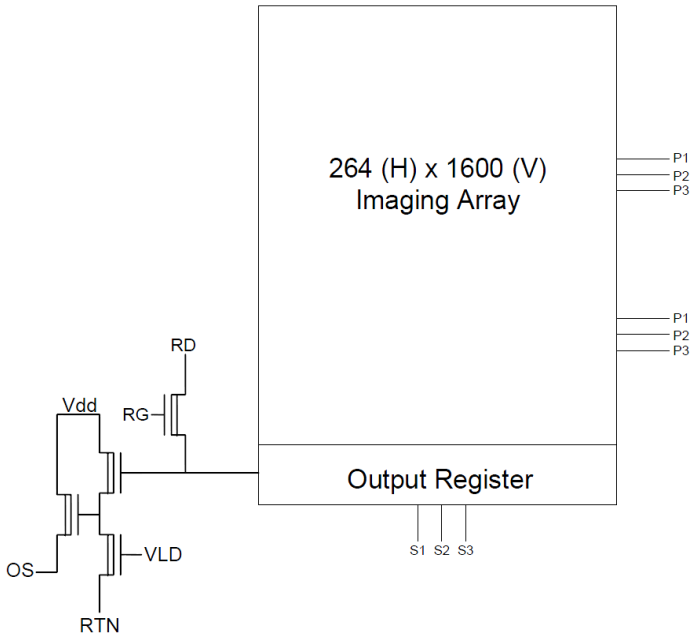
The output amplifier drains are tied to OD. The source (OS) is connected to an external load resistor to ground and constitutes the video output from the device. The output voltage changes linearly in response to the number of electrons delivered to the sense node.

Timing Diagram

Full device:



Individual section:



DC Operating Characteristics

Symbol	Parameter	Range min	Range nom	Range max	Unit	Remarks
OD	DC Supply Voltage	20.0	24.0	30.0	V	
RD	Reset Drain Voltage	10.0	15.0	20.0	V	
OTG	Output Transfer Gate Voltage	-5.0	-1.0	5.0	V	
Vss	Substrate Ground		0.0		V	

Typical Clock Voltages

Symbol	Parameter	High	Low	Unit	Remarks
S1,S2,S3	Horizontal Serial Clocks	+5.0	-5.0	V	Typical clock range
SW	Summing Gate Clock	+5.0	-5.0	V	Clock as S2 if not clocked separately
A1,A2,A3	Vertical Array Clocks	+3.0	-9.0	V	
RG	Reset Gate Array Clock	+8.0	0.0	V	

AC Characteristics

Symbol	Parameter	Range min	Range nom	Range max	Unit	Remarks
V_{ODC}	Output DC Level		14.0		V	Typical
Zsingle	Suggested Load Register	1.0	2.0	20.0	kΩ	Higher resistance reduces bandwidth

Performance Specifications

Symbol	Parameter	Range min	Range nom	Range max	Unit	Remarks
V_{SAT}	Saturation Output Voltage Full Well Capacity	750 60k		90K	mV e-	
	Output amplifier sensitivity	7.0			µV/e-	
PRNU	Photo Response Non-Uniformity Peak-to-Peak			10	$\%V_{SAT}$	
DSNU	Dark Signal Non-Uniformity Peak-to-Peak			1.0	mV	
CTE	Charge Transfer Efficiency	>0.999995				
DC	Dark Current	1.0			e-/pix/sec	25°C
	Output Linearity	<2%				
N_{RMS}	Readout Noise	20	30	40	e-	20MHz

Cosmetic Grading

Grading and screening of devices establishes a ranking for the image quality that a CCD provides. Blemishes are characterized as spurious pixels exceeding 10% of V_{SAT} with respect to neighboring elements. Blemish content is determined in the dark, at various illumination levels, and for different device temperatures.

The CCD2520A CCD image sensor is available in various standard grades, as well as custom grades. Consult ANDANTA GmbH for information on grade selection.

Warranty

ANDANTA GmbH will repair or replace, at our option, any image sensor product within twelve months of delivery to the end customer, for any defect in materials or workmanship. Contact ANDANTA GmbH for further warranty information, a return number, and shipping instructions

Certification

ANDANTA GmbH certifies that all products are carefully inspected and tested prior to shipment and will meet all of the specification requirements under the performance specifications summarized.

ANDANTA GmbH Detektortechnologie
Ilzweg 7+9 • 82140 Olching/Deutschland
Tel: +49 8142 41058-0 • Fax: +49 8142 41058-29
e-mail: epost@andanta.de • www.andanta.de