CCD1630A/CCD1632A
1330 x 1320 Element Image Area
Full Frame CCD Image Sensor

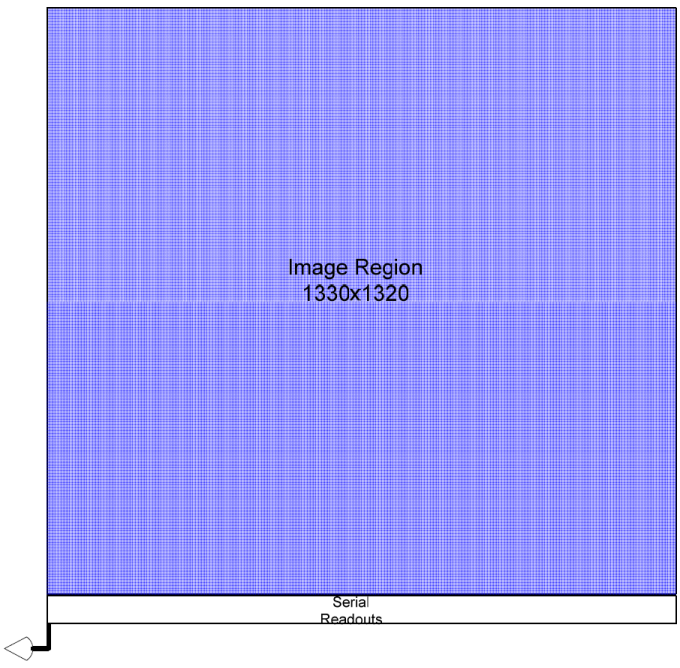
Features

- 1330 x 1320 Photosite Full Frame CCD Array
- 9 µm x 9 µm Pixel
- 12.06mm x 11.88mm Image Area
- 100% Fill Factor
- Readout Noise Less Than 30 Electrons at 20MHz
- Dynamic Range > 70dB @20Mhz
- 1 Two Stage Source Follower Output Channels
- Three-Phase Buried Channel NMOS Image area
- Three-Phase Buried Channel Readout Registers
- Multi-Pinned Phase (MPP) optional

General Description

The CCD1630 is a 1330 x 1320 image element solid state Charge Coupled Device (CCD) Full Frame sensor.

This CCD is intended for use in high-resolution scientific, space based, industrial, and commercial electro-optical systems. The CCD1630 is organized in a single array of 1330 horizontal by 1320 vertical photosites. The pixel spacing is 9µm x 9µm. For dark reference, each readout line is proceeded by 8 dark pixels. This imager is available in a full frame transfer configuration (shown). The CCD1630 is offered in an MPP mode frontside illuminated version for decreased dark signal.



Single 20 Mhz Output

Functional Description

The following functional elements are illustrated in the block diagram:

Image Sensing Elements: Incident photons pass through a transparent polycrystalline silicon gate structure creating electron hole pairs. The resulting photoelectrons are collected in the photosites during the integration period. The amount of charge accumulated in each photosite is a linear function of the localized incident illumination intensity and integration period.

The photosite structure is made up of contiguous CCD elements with no voids or inactive areas. In addition to sensing light, these elements are used to shift image data vertically. Consequently, the device needs to be shuttered during readout.

Vertical Charge Shifting: The Full Frame architecture of the CCD1630 provides video information as a single sequential readout of 1320 lines containing 1330 photosites. At the end of an integration period the ϕV1, ϕV2, and ϕV3 clocks are used to transfer charge vertically through the CCD array to the horizontal readout register. Vertical columns are separated by a channel stop region to prevent charge migration.

Horizontal Charge Shifting: ϕH1, ϕH2 and ϕH3 are polysilicon gates used to transfer charge horizontally to the output amplifier. The horizontal transport register is twice the size of the photosite to allow for vertical binning. For both frame transfer configurations, the charge may be read out through the eight amplifiers at the bottom or top of the image frame storage region

The transfer of charge into the horizontal register is the result of a vertical shift sequence. This register has 8 additional register cells between the first pixel of each line and the output amplifier. The output from these locations contains no signal and may be used as a dark level reference.

The last clocked gate in the Horizontal registers is twice as large as the others and can be used to horizontally bin charge. This gate requires its own clock, which may be tied to ϕH2 for normal full resolution readout.

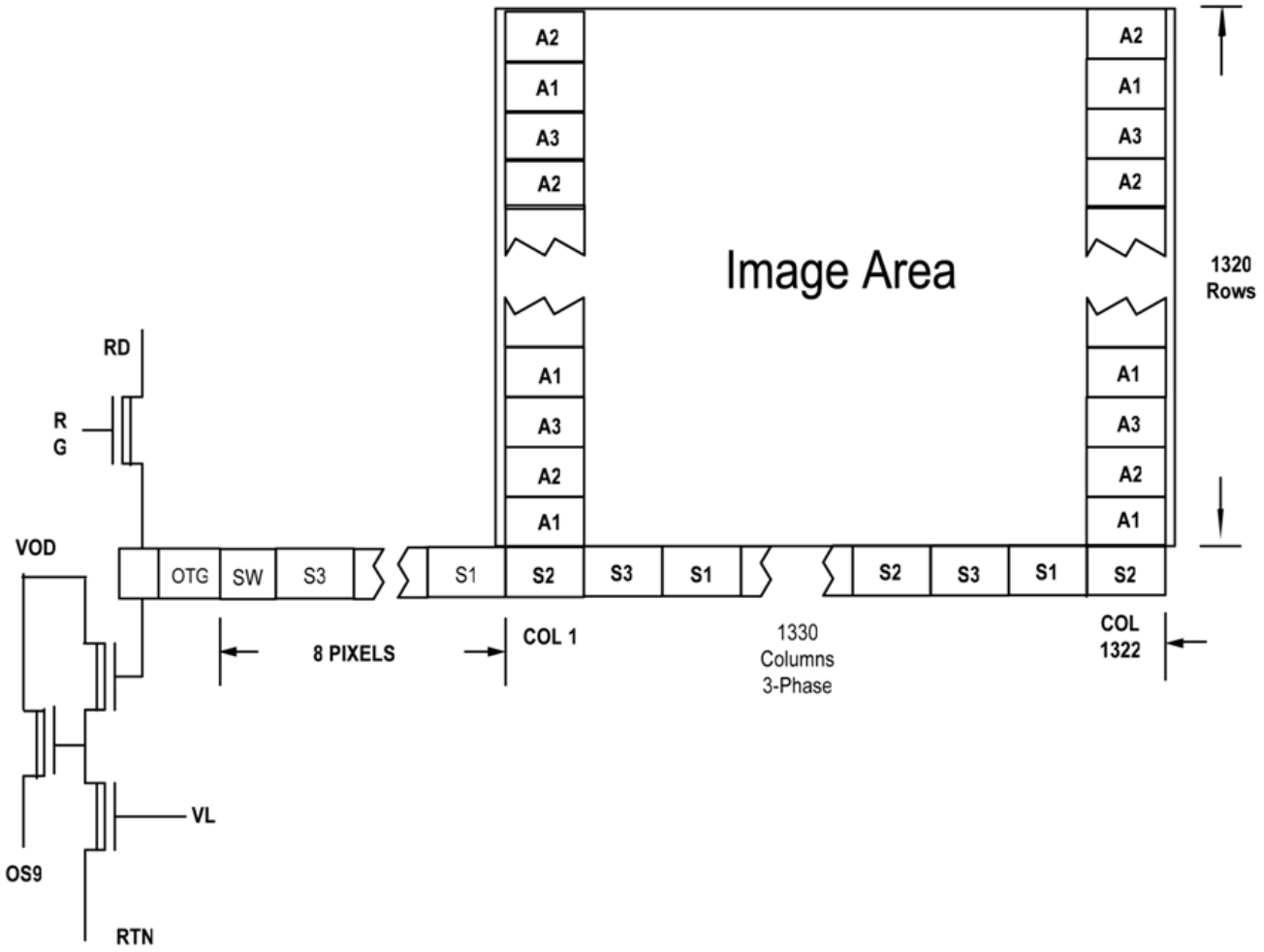
The reset FET in the horizontal readout, clocked appropriately with ϕR, allows binning of adjacent pixels.

Output Amplifier: The CCD1630 has one output amplifier at the end the single Horizontal register. They are dual FET floating diffusion amplifiers with a reset MOSFET tied to the input gate.

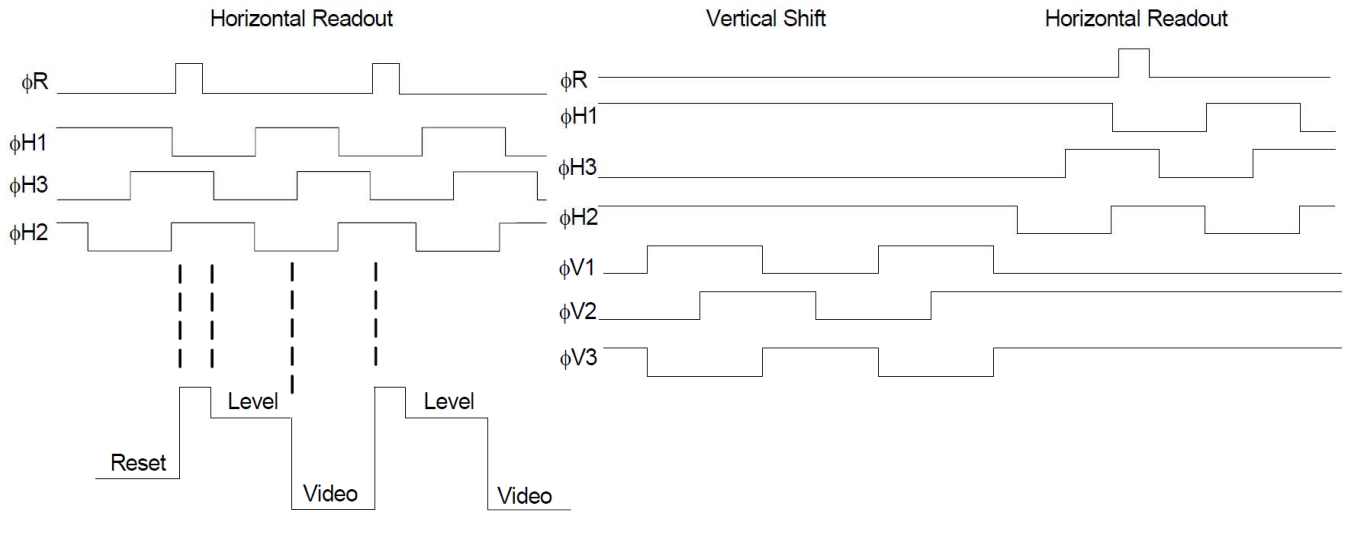
Charge packets are clocked to a pre-charged capacitor whose potential changes linearly in response to the number of electrons delivered. When this potential is applied to the input gate of an NMOS amplifier, a signal at the output V_{out} pin is produced. The capacitor is then reset via the reset MOSFET with ϕR to a pre-charge level prior to the arrival of the next charge packet except when horizontally binning. The output amplifier drain is tied to VDD.

The source is connected to an external load resistor to ground and constitutes the video output from the device.

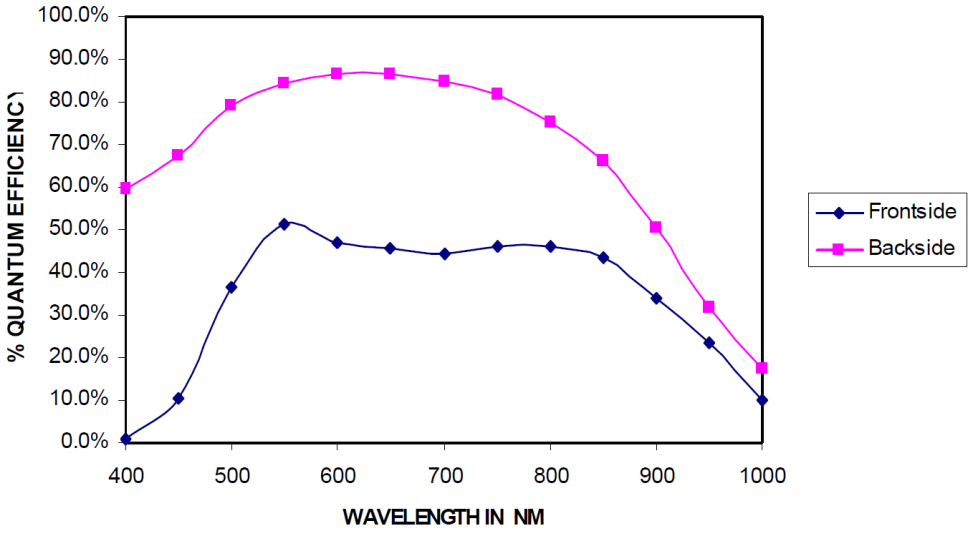
CCD 1630 Image Readout Section



Timing Diagram



Typical CCD Quantum Efficiency



Definition of Terms

Charge-Coupled Device	A charge-coupled device is a monolithic silicon structure in which discrete packets of electron charge are transported from position to position by sequential clocking of an array of gates.
Vertical Transport Clocks	ϕV1, ϕV2, ϕV3 the clock signals applied to the vertical transport register. The nomenclature used is A1, A2, and A3.
Horizontal Transport Clocks	ϕH1, ϕH2, ϕH3 the clock signals applied to the horizontal transport registers. The nomenclature used is S1, S2, and S3.
Reset Clock	ϕR the clock applied to the reset switch of the output amplifier.
Dynamic Range	The ratio of saturation output voltage to RMS noise in the dark. The peak-to-peak random noise is 4-6 times the RMS noise output.
Saturation Exposure	The minimum exposure level that produces an output signal corresponding to the maximum photosite charge capacity. Exposure is equal to the product of light intensity and integration time.
Responsivity	The output signal voltage per unit of exposure.
Spectral Response Range	The spectral band over which the response per unit of radiant power is more than 10% of the peak response.
Photo-Response Non-Uniformity	The difference of the response levels between the most and the least sensitive regions under uniform illumination (excluding blemished elements) expressed as a percentage of the average response.
Dark Signal	The output signal is caused by thermally generated electrons. Dark signal is a linear function of integration time and an exponential function of chip temperature.
Vertical Transfer Gate ϕVTG	Gate structures adjacent to the end row of photosites and the horizontal transport registers. The charge packets accumulated in the photosites are shifted vertically through the array. Upon reaching the end row of photosites, the charge is transferred in parallel via the transfer gates to the horizontal transport shift registers whenever the transfer gate voltage goes low.
Pixel	Picture element or sensor element, also called photo element or photosite

DC Operating Characteristics

Symbol	Parameter	Range min	Range nom	Range max	Unit	Remarks
V_{DD}	DC Supply Voltage		25.0		V	
V_{RD}	Reset Drain Voltage		16.0		V	
V_{OG}	Output Voltage	-2.0	1.0	2.0	V	
V_{SS}	Substrate Ground		0.0		V	
V_{SC}	Scupper		23.0		V	

Typical Clock Voltages

Symbol	Parameter	High	Low	Unit	Remarks
VϕH(1,2)	Horizontal Multiplexer Clock	+5.0	-5.0	V	Note 1
VϕSG	Summing Gate Clock	+5.0	-5.0	V	Note 1
VϕV(1,2,3,4)	Vertical Array Clocks	+3.0	-10.0	V	Note 1
VϕR	Reset Array Clock	+5.0	-5.0	V	Note 1

Note 1: ϕH = 200pF, ϕV = 15,000pF. All clock rise and fall times should be > 10 ns.

AC Characteristics

Symbol	Parameter	Range min	Range nom	Range max	Unit	Remarks
V_{ODC}	Output DC Level		17.0		V	
Z	Suggested Load Register	1.0	5.0	20.0	kΩ	

Standard test conditions are nominal MPP clocks and DC operating Voltages, 1 MHz Horizontal Data Rate, 6µSec Vertical shift cycle.

Performance Specifications

Symbol	Parameter	Range min	Range nom	Range max	Unit	Remarks
V_{SAT}	Saturation Output Voltage Full Well Capacity Output Amp Sensitivity	70K	700 80K 8.0	100K	mV e- µV/e-	Note 1
PRNU	Photo Response Non-Uniformity Peak-to-Peak		10		$\%V_{SAT}$	
DSNU	Dark Signal Non-Uniformity Peak-to-Peak			1.0	mV	
DC	Dark Current	0.025	<1.0	2.0	nA/cm^2	Note 2
R	Responsivity		1.0		$Vµj/cm^2$	
rms	Noise		5 -20		e^-	

Note 1: Maximum well capacity is achieved in Buried Channel Mode.
Note 2: Values shown are for 250C. Dark current doubles for every 50- 70C.

Quantum Efficiency Enhancements

The CCD1630 CCD area arrays can be backside thinned for increased QE. The incident illumination enters through the backside of the array, and since no photons are absorbed in the polysilicon gate structures, the QE is increased. Also available are front side illuminated devices which can be coated with a fluorescent dye that absorbs UV light and fluoresces in the visible range. This provides CCD response at wavelengths less than 400nm.

Cosmetic Grading

Device grading helps to establish a ranking for the image quality that a CCD will provide. Blemishes are characterized as spurious pixels exceeding 10% of V_{SAT} with respect to neighboring elements. Blemish content is determined in the dark, at various illumination levels, and for different device temperatures.

The CCD1630 is available in various standard grades, as well as custom selected grades.

Consult ANDANTA GmbH for available grading information and custom selections.

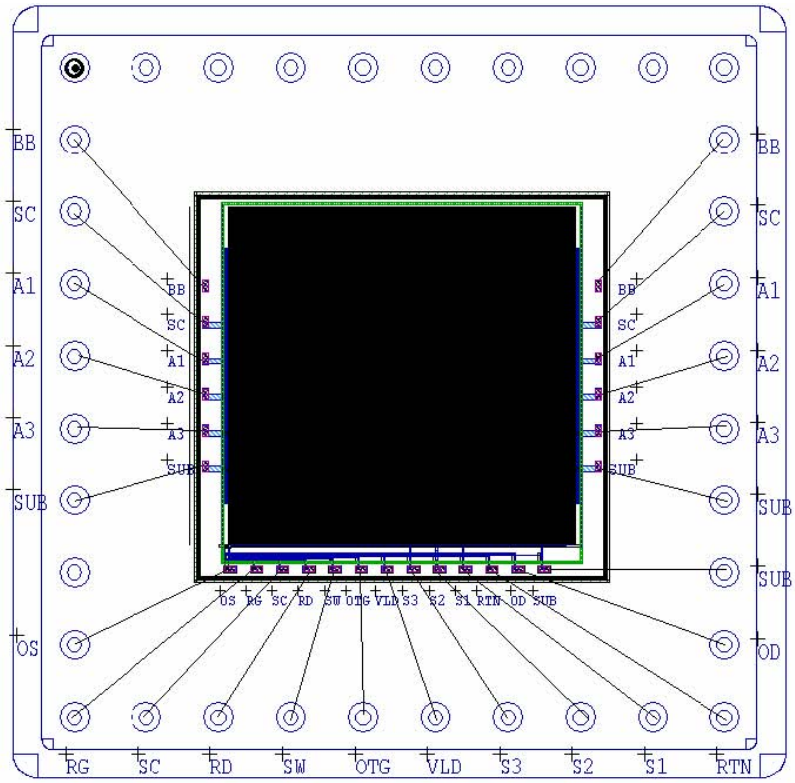
Warranty

Within twelve months of delivery to the end customer ANDANTA GmbH will repair or replace, at our option, any image sensor product if any part is found to be defective in materials or workmanship. Contact ANDANTA GmbH for assignment of warranty return number and shipping instructions to ensure prompt repair or replacement.

Certification

ANDANTA GmbH certifies that all products are carefully inspected and tested prior to shipment and will meet all of the specification requirements under which it is furnished

CCD1630A/32A Package



1	NC	13	A1	25	SW
2	NC	14	A2	26	RD
3	NC	15	A3	27	SC
4	NC	16	SUB	28	RG
5	NC	17	SUB	29	OS
6	NC	18	OD	30	NC
7	NC	19	RTN	31	SUB
8	NC	20	S1	32	A3
9	NC	21	S2	33	A2
10	NC	22	S3	34	A1
11	BB	23	VLD	35	SC
12	SC	24	OTG	36	BB

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